

# 2011 International Conference on Reconfigurable Computing and FGAs, ReConFig11

## Conference Program

Tuesday - November 29									
17:00 - 19:00	Registration								
Wednesday - November 30									
08:30 - 18:00	Registration								
09:00 - 10:00	Keynote #1: " <b>Accelerating Innovation and Discovery with Graphical System Design and Reconfigurable Processing Platforms</b> " by <b>Dr. James Truchard</b> , National Instruments' president & CEO								
10:00 - 10:15	Break								
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Thursday - December 1		
08:30 - 16:00	Registration	
09:00 - 10:00	Keynote #2: "An Introduction to Tabula's Spacetime Architecture" by Dr. Brad Hutchings, Tabula, Inc.	
10:00 - 10:15	Break	
10:15 - 11:30	<b>Session 4A - General Session</b>	<b>Session 4B - Reconfiguration Techniques</b>
	4A_1: "Multi-stream Regular Expression Matching on FPGA", Qu Yun, Yi-Hua E. Yang, Viktor K. Prasanna.	4B_1: "A Self-Configuring TMR Scheme utilizing Discrepancy Resolution", Naveed Imran, Ronald F. DeMara.
	4A_2: "Object Recognition on a Chip: A Complete SURF-Based System on a Single FPGA", Michael Schaeferling, Gundolf Kiefer.	4B_2: "Power centric application mapping for Dynamically Reconfigurable Processor Array with DualVdd and DualVth", Kazuei Hironaka, Hideharu Amano.
	<b>Introduction to Poster Session C</b>	<b>Introduction to Poster Session D</b>
11:30 - 12:00	Break - Poster Sessions C & D	
12:00 - 13:15	<b>Session 5A - Reconfigurable Computing for DSP and Communications</b>	<b>Session 5B - High Performance Reconfigurable Computing</b>
	5A_1: "Architecture Based on Array Processors for Data-Dependent Superimposed Training Channel Estimation", Eduardo Romero Aguirre, Ramón Parra Michel, Roberto Carrasco Alvarez, Aldo Gustavo Orozco Lugo.	5B_1: "Optimizing Decomposition-based Packet Classification Implementation on FPGAs", Lu Sun, Hoang Le, Viktor K. Prasanna.
	5A_2: "Adaptive Energy-efficient Architecture for WCDMA Channel Estimation", Zoltan E. Rakosi, Zheng Wang, Anupam Chattopadhyay.	5B_2: "Dynamic Constant Reconfiguration for Explicit Finite Difference Option Pricing", Tobias Becker, Qiwei Jin, Wayne Luk, Stephen Weston.
	5A_3: "High-Speed Stochastic Processes Generator based on Sum-of-Sinusoids for Channel Emulation", Luia Rene Vela Garcia, Javier Vazquez Castillo, Ramon Parra Michel, Alejandro Castillo Atoche.	5B_3: "Snake: An Efficient Strategy for the Reuse of Circuitry and Partial Computation Results in High-Performance Reconfigurable Computing", Xabier Iturbe, Khaled Benkruid, Ali Ebrahim, Chuan Hong, Tughrul Arslan, Imanol Martinez.
13:15 - 15:00	Lunch	
15:00 - 16:15	<b>Session 6A - Reconfigurable Computing for Security and Cryptography</b>	<b>Session 6B - General Session</b>
	6A_1: "A Precharge-Absorbed DPL Logic for Reducing Early Propagation Effects on FPGA Implementations", Wei He, Eduardo de la Torre, Teresa Riesgo.	6B_1: "Measuring and Predicting Temperature Distributions on FPGAs at Run-Time", Markus Happe, Andreas Agne, Christian Plessl.
	6A_2: "Pseudo-LFSR PUF: A Compact, Efficient and Reliable Physical Unclonable Function", Yohei Hori, Hyunho Kang, Toshihiro Katashita, Akashi Satoh.	6B_2: "Heterogeneous Concurrent Error Detection (hCED) Based on Output Anticipation", Naveed Imran, Ronald F. DeMara.
	6A_3: "Hardware Design of A 256-bit Prime Field Multiplier Suitable for Computing Bilinear Pairings", Cuautémoc Chávez Corona, Edgar Ferrer Moreno, Francisco Rodríguez Henríquez.	6B_3: "Configuring Field-Programmable Robot Arrays", Mark G. Arnold.
16:45-23:30	Trip to Playa del Carmen & Conference Dinner	

Friday - December 2											
08:30 - 15:00	Registration										
09:00 - 10:00	Keynote #3: "Reconfigurable Computing: What happens when you start at the requirements stage?" by Dr. Steve Kelem, ElementCXI, Inc.										
10:00 - 10:15	Break										
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16:40 - 16:45	Closing										

Poster Session A	Poster Session B
PA_1: "Robustness analysis of different AES implementations on SRAM based FPGAs", Uli Kretzschmar, Armando Astarloa, Jesús Lázaro, Unai Bidarte, Jaime Jimenez.	PB_1: "Techniques for Dynamically Mapping Computations to Coprocessors", João Carlos Viegas Marting Bispo, João M. P. Cardoso.
PA_2: "Efficient Dual-Rail Implementations in FPGA using Block RAMs", Shivam Bhasin, Sylvain Guilley, Youssef Souissi, Tarik Graba, Jean-Luc DANGER.	PB_2: "Rainbow - An OS Extension for Hardware Multitasking on Dynamically Partially Reconfigurable FPGAs", Krzysztof Jozwik, Hiroyuki Tomiyama, Masato Edahiro, Shinya Honda, Hiroaki Takada.
PA_3: "Versatile FPGA Architecture for Skein Hashing Algorithm", David M. Webster, Marcin Lukowiak.	PB_3: "Scalable Models for Autonomous Self-Assembled Reconfigurable Systems", Teresa G. Cervero, Sebastián López, Roberto Sarmiento, Tannous Frangieh, Peter Athanas.
PA_4: "GPU vs FPGA: Example Application on White Light Interferometry", Alexander Pacholik, Marcus Müller, Wolfgang Fengler, Torsten Machleidt, Karl-Heinz Franke.	PB_4: "LiSARD: LabVIEW Integrated Softcore Architecture for Reconfigurable Devices", Alexander Pacholik, Johannes Klöckner, Marcus Müller, Irina Gushchina, Wolfgang Fengler.
PA_5: "Spectral Method Characterization on FPGA and GPU Accelerators", Karl Savio Pimenta Pereira, Peter Athanas, Heshan Lin, Wu Feng.	PB_5: "EDA Environment for Evaluating a New Switch-Block-Free Reconfigurable Architecture", Masatoshi Nakamura, Masato Inagi, Kazuya Tanigawa, Tetsuo Hironaka, Masayuki Sato, Takashi Ishiguro.

Poster Session C	Poster Session D
PC_1: "Fixed-Point CORDIC-Based QR Decomposition by Givens Rotations on FPGA", Dongdong CHEN, Mihai SIMA.	PD_1: "A Coarse-Grained Reconfigurable Processor for Sequencing and Phylogenetic Algorithms in Bioinformatics", Pei Liu, Fatemeh Ostad Ebrahim, Kolin Paul, Ahmed Hemani.
PC_2: "Analysis of Parallel Sorting Algorithms in K-best Sphere-Decoder Architectures for MIMO Systems", Pedro Cervantes-Lozano, Luis Fernando González-Pérez, Andrés David García-García.	PD_2: "Reconfigurable Block Floating Point Processing Elements in Virtex Platforms", Guillermo Conde, Gregory W. Donohoe.
PC_3: "Design and Implementation of a simplified Turbo Decoder for 3GPP2", Lennin Conrado Yllescas-Calderón, Joaquin Adrian Espino-Orozco, Ramon Parra-Michel, Luis Fernando González-Pérez.	PD_3: "Digital Talking Book Player for the Visually Impaired Using FPGAs", Azadeh Nazemi, Cesar Ortega-Sanchez, Iain Murray.
PC_4: "Arbitrary Distribution Random Variable Generator for Channel Emulators", Rosalba del Refugio Zarate Martinez, Fernando Peña Campos, Javier Vazquez Castillo.	PD_4: "Using Self-Reconfiguration to Increase Manufacturing Yield of CNTFET-Based Architectures", Hui Zhu, Sébastien Le Beux, Nataliya Yakymets, Ian O'Connor.
PC_5: "Performance-Area Improvement by Partial Reconfiguration for an Aerospace Remote Sensing Application", Luis Andres Cardona, Jharna Agrawal, Yi Guo, Joan Oliver, Carles Ferrer.	PD_5: "Hardware OS Communication Service and Dynamic Memory Management for RSoCs", Surya Narayanan, Daniel Chillet, Sebastien Pillement, Ioannis Sourdis.
PC_6: "Reconfigurable FPGA-Based Unit for Singular Value Decomposition of Large $m \times n$ Matrices", Luis M. Ledesma-Carrillo, Eduardo Cabal-Yepez, Rene de J. Romero-Troncoso, Arturo Garcia-Perez, Roque A. Osornio-Rios, Tobia D. Carozzi.	PD_6: "Dynamic processor reconfiguration", M. Hübner, C. Tradowsky, D. Göhringer, L. Braun, F. Thoma, J. Henkel, J. Becker.

Poster Session E	Poster Session F
PE_1: "GIMME - A General Image Multiview Manipulation Engine", Carl Ahlberg, Jörgen Lidholm, Fredrik Ekstrand, Giacomo Spampinato, Mikael Ekström, Lars Asplund.	PF_1: "Toward all optical interconnections in chip Multiprocessor", Malek Channoufi, Pierre Lecoy, Rabah Attia, Bruno Delacressoniere.
PE_2: "Low-Cost TMR for Fault-Tolerance on Coarse-Grained Reconfigurable Architectures", Thomas Schweizer, Philipp Schlicker, Sven Eisenhardt, Tommy Kuhn, Wolfgang Rosenstiel.	PF_2: "Network on Chip Architectures for High Performance Digital Signal Processing Using a Configurable Core", Juan Carlos Pena Ramos, Ramon Parra Michel.
PE_3: "A PID Controller Applied to the Gain Control of a CMOS Camera Using Reconfigurable Computing", Drausio Linardi Rossi, João Miguel Gago Pontes de Brito Lima, Vanderlei Bonato, Eduardo Marques.	PF_3: "Enhancing the Randomness of a Combined True Random Number Generator Based on the Ring Oscillator Sampling Method", Mieczyslaw Jessa, Lukasz Matuszewski.
PE_4: "FPGA Based Acceleration of Decimal Operations", Alberto Nannarelli.	PF_4: "RAM-Based Ultra-Lightweight FPGA Implementation of PRESENT", Elif Bilge Kavun, Tolga Yalcin.
PE_5: "MiniMIPS: An 8-Bit MIPS in an FPGA for Educational Purposes", Cesar Ortega-Sanchez.	PF_5: "Fault Tolerance Analysis and Self-Healing Strategy of Autonomous, Evolvable Hardware Systems", Ruben Salvador, Andres Otero, Javier Mora, Eduardo de la Torre, Lukáš Sekanina, Teresa Riesgo.
PE_5: "Linking Formal Description and Simulation of Runtime Reconfigurable Systems", Thilo Pionteck, Christoph Osterloh, Carsten Albrecht.	