2011 International Conference on Reconfigurable Computing and FGAs, ReConFig11

Conference Program

Tuesday - November 29	
17:00 - 19:00	Registration

Wednesday - November 30		
08:30 - 18:00	Registration	
09:00 - 10:00	Keynote #1: "**Accelerating Innovation and Discovery with Graphical System Design and Reconfigurable Processing Platforms**" by **Dr. James Truchard**, National Instruments' president & CEO	
10:00 - 10:15	Break	
10:15 - 11:30	**Session 1A - General Session**	**Session 1B - Reconfigurable Computing for DSP and Communications**
	1A_1: "An Analysis of Implanted Antennas in Xilinx FPGAs", Jacob Couch, Peter Athanas.	1B_1: "A Simple Ethernet Stack Implementation in VHDL to Enable FPGA logic reconfigurability", Marcus R Perrett, Izzat Darwazeh.
	1A_2: "Adaptive Multi-Client Network-on-Chip Memory", Diana Goehringer, Lukas Meder, Michael Huebner, Juergen Becker.	1B_2: "FPGA-based CPG robot locomotion modulation using a fuzzy scheme and visual information", Jose Hugo Barron-Zambrano, Cesar Torres-Huitzil, Jose Juan Garcia-Hernandez.
	1A_3: "FPGA Implementations of Radix-10 Digit Recurrence Fixed-Point and Floating-Point Dividers", Malte Baesler, Sven-Ole Voigt, Thomas Teufel.	1B_3: "Improving KLT in Embedded Systems by Processing Oversampling Video Sequence in Real-time", Zhilei Chai, Jianbo Shi.
11:30 - 12:00	Break	
12:00 - 13:15	**Session 2A - General Session**	**Session 2B - Multiprocessor Systems and Networks on Chip**
	2A_1: "Configuration Bitstream Reduction for SRAM-based FPGAs by Enumerating LUT Input Permutations", Ameer Abdelhadi, Guy G. F. Lemieux.	2B_1: "Reconfigurable Systems and Flexible Programming for Hardware Design, Verification and Software Enablement for System-on-a-Chip Architectures", John Aylward, Catherine H. Crawford, Ken Inoue, Scott Lekuch, Kay Muller, Mark Nutter, Hartmut Penner, Kai Schleupen, Jimi Xenidis.
	2A_2: "Empty Resource Compaction Algorithms for Real-Time Hardware Tasks Placement on Partially Reconfigurable FPGAs Subject to Fault Ocurrence", Xabier Iturbe, Khaled Benkrid, Tughrul Arslan, Chuan Hong, Imanol Martinez.	2B_2:" Open-Scale: A Scalable, Open-Source NOC-Based MPSoC for Design Space Exploration", Remi Busseuil, Lyonel Barthe, Gabriel Marchesan Almeida, Luciano Ost, Florent Bruguier, Gilles Sassatelli, Pascal Benoit, Michel Robert, Lionel Torres.
	2A_3: "Resource Efficient Arithmetic Effects on RBM Neural Network Solution Quality Using MNIST", Antony W. Savich, Medhat Moussa.	2B_3: "Improving Fault Tolerance of Network-on-Chip Links via Minimal Redundancy and Reconfiguration", Hamed Sajjadi Kia, Cristinel Ababei.
13:15 - 15:00	Lunch	
15:00 - 16:15	**Session 3A - "Reconfigurable Computing for Security and Cryptography", Chair:**	**Session 3B - Reconfiguration Techniques**
	3A_1: "An Integrated Prime-field ECDLP Hardware Accelerator with High-performance Modular Arithmetic Units", Suvarna Mane, Lyndon Judge, Patrick Schaumont.	3B_1: "FPGA Bootstrapping on PCIe Using Partial Reconfiguration", Patrick S. Ostler, Michael J. Wirthlin,, Joshua E. Jensen.
	3A_2: "MicroECC: A Lightweight Reconfigurable Elliptic Curve Crypto-Processor", Michal Varchola, Tim Guneysu, Oliver Mischke.	3B_2: "From Instruction Traces to Specialized Reconfigurable Arrays", João Carlos Viegas Marting Bispo, Nuno Paulino, João M. P. Cardoso, João Canas Ferreira.
	3A_3: "dcTPM: A Generic Architecture for Dynamic Context Management", Thomas Feller, Sunil Malipatlolla, Michael Kasper, Sorin A. Huss.	3B_3: "Towards Symbolic Run-Time Reconfiguration in Tightly-Coupled Processor Arrays", Srinivas Boppu, Frank Hannig, Jürgen Teich, José Roberto Pérez Andrade.
16:15 - 16:50	**Introduction to Poster Session A**	**Introduction to Poster Session B**
16:50 - 17:20	Break - Poster Session A & B	
17:20 - 18:30	Discussion Panel	
20:00 - 22:00	Welcome Cocktail & Demo Night	

Thursday - December 1		
08:30 - 16:00	Registration	
09:00 - 10:00	Keynote #2: "**An Introduction to Tabula's Spacetime Architecture**" by **Dr. Brad Hutchings**, Tabula, Inc.	
10:00 - 10:15	Break	
10:15 - 11:30	**Session 4A - General Session**	**Session 4B - Reconfiguration Techniques**
	4A_1: "Multi-stream Regular Expression Matching on FPGA", Qu Yun, Yi-Hua E. Yang, Viktor K. Prasanna.	4B_1: "A Self-Configuring TMR Scheme utilizing Discrepancy Resolution", Naveed Imran, Ronald F. DeMara.
	4A_2: "Object Recognition on a Chip: A Complete SURF-Based System on a Single FPGA", Michael Schaeferling, Gundolf Kiefer.	4B_2: "Power centric application mapping for Dynamically Reconfigurable Processor Array with DualVdd and DualVth", Kazuei Hironaka, Hideharu Amano.
	Introduction to Poster Session C	**Introduction to Poster Session D**
11:30 - 12:00	Break - Poster Sessions C & D	
12:00 - 13:15	**Session 5A - Reconfigurable Computing for DSP and Communications**	**Session 5B - High Performance Reconfigurable Computing**
	5A_1: "Architecture Based on Array Processors for Data-Dependent Superimposed Training Channel Estimation", Eduardo Romero Aguirre, Ramón Parra Michel, Roberto Carrasco Alvarez, Aldo Gustavo Orozco Lugo.	5B_1: "Optimizing Decomposition-based Packet Classification Implementation on FPGAs", Lu Sun, Hoang Le, Viktor K. Prasanna.
	5A_2: "Adaptive Energy-efficient Architecture for WCDMA Channel Estimation", Zoltan E. Rakosi, Zheng Wang, Anupam Chattopadhyay.	5B_2: "Dynamic Constant Reconfiguration for Explicit Finite Difference Option Pricing", Tobias Becker, Qiwei Jin, Wayne Luk, Stephen Weston.
	5A_3: "High-Speed Stochastic Processes Generator based on Sum-of-Sinusoids for Channel Emulation", Luia Rene Vela Garcia, Javier Vazquez Castillo, Ramon Parra Michel, Alejandro Castillo Atoche.	5B_3: "Snake: An Efficient Strategy for the Reuse of Circuitry and Partial Computation Results in High-Performance Reconfigurable Computing", Xabier Iturbe, Khaled Benkrid, Ali Ebrahim, Chuan Hong, Tughrul Arslan, Imanol Martinez.
13:15 - 15:00	Lunch	
15:00 - 16:15	**Session 6A - Reconfigurable Computing for Security and Cryptography**	**Session 6B - General Session**
	6A_1: "A Precharge-Absorbed DPL Logic for Reducing Early Propagation Effects on FPGA Implementations", Wei He, Eduardo de la Torre, Teresa Riesgo.	6B_1: "Measuring and Predicting Temperature Distributions on FPGAs at Run-Time", Markus Happe, Andreas Agne, Christian Plessl.
	6A_2: "Pseudo-LFSR PUF: A Compact, Efficient and Reliable Physical Unclonable Function", Yohei Hori, Hyunho Kang, Toshihiro Katashita, Akashi Satoh.	6B_2: "Heterogeneous Concurrent Error Detection (hCED) Based on Output Anticipation", Naveed Imran, Ronald F. DeMara.
	6A_3: "Hardware Design of A 256-bit Prime Field Multiplier Suitable for Computing Bilinear Pairings", Cuautémoc Chávez Corona, Edgar Ferrer Moreno, Francisco Rodríguez Henríquez.	6B_3: "Configuring Field-Programmable Robot Arrays", Mark G. Arnold.
16:45-23:30	Trip to Playa del Carmen & Conference Dinner	

	Friday - December 2	
08:30 - 15:00	Registration	
09:00 - 10:00	Keynote #3: "**Reconfigurable Computing: What happens when you start at the requirements stage?**" by **Dr. Steve Kelem**, ElementCXI, Inc.	
10:00 - 10:15	Break	
10:15 - 11:30	**Session 7A - General Session**	**Session 7B - Multiprocessor Systems and Networks on Chip**
	7A_1: "Identifying Merge-Beneficial Software Kernels for Hardware Implementation", Adriano Kaminski Sanches, João M. P. Cardoso, Alexandre C. B. Delbem.	7B_1: "The Impact of Global Routing on the Performance of NoCs in FPGAs", Ye Lu; John McCanny; Sakir Sezer.
	7A_2: "A Reconfigurable Computing System Based on a Cache-Coherent Fabric", Neal Oliver, Rahul R Sharma, Stephen Chang, Bhushan Chitlur, Elkin Garcia, Joseph Grecco, Aaron Grier, Nelson Ijih, Yaping Liu, Pratik Marolia, Henry Mitchel, Suchit Subhaschandra, Arthur Sheiman, Tim Whisonant,, Prabhat Gupta.	7B_2: "Automatic Type Inference for Resynthesis on Hardware Description Languages", Germán León, José M. Claver, Germán Fabregat.
	Introduction to Poster Session E	**Introduction to Poster Session F**
11:30-12:00	Break - Poster sessions E & F	
12:00 - 13:15	**Session 8A - Controversy track: FPGAs Vs GPUs**	**Session 8B - Reconfigurable Computing for Security and Cryptography**
	8A_1: "Enumeration of Costas arrays using GPUs and FPGAs", Rafael Arce-Nazario, Jose R. Ortiz-Ubarri.	8B_1: "Area-efficient FPGA Implementations of the SHA-3 Finalists", Bernhard Jungk, Jürgen Apfelbeck.
	8A_2: "An Energy Efficient FPGA Accelerator for Monte Carlo Option Pricing with the Heston Model", Christian de Schryver, Ivan Shcherbakov, Frank Kienle, Norbert Wehn, Henning Marxen, Anton Kostiuk, Ralf Korn.	8B_2: "Efficient Hardware Accelerator for IPSec based on Partial Reconfiguration on Xilinx FPGAs", Ahmad Salman, Marcin Rogawski, Jens-Peter Kaps.
	8A_3: "Highly Parameterized K-means Clustering on FPGAs: Comparative Results with GPPs and GPUs", Hanaa M. Hussain, Khaled Benkrid, Ahmet T.Erdogan, Huseyin Seker.	8B_3: "Decrypting HDCP-Protected Video Streams using Reconfigurable Hardware", Benno Lomb, Tim Güneysu.
13:15 - 15:00	Lunch	
15:00 - 16:40	**Session 9A - General Session**	**Session 9B - Productivity Environments and High Level Languages**
	9A_1: "Deterministic Timing-Driven Parallel Placement by Simulated Annealing using Half-Box Window Decomposition", Jeffrey B. Goeders, Steven J.E. Wilton, Guy G.F. Lemieux.	9B_1: "Improving FPGA Design and Evaluation Productivity with a Hardware Performance Monitoring Infrastructure", Andrew G. Schmidt, Ron Sass.
	9A_2: "Characterizing non-Ideal Impacts of Reconfigurable Hardware Workloads on Ring Oscillator-based Thermometers", Moinuddin A Sayed, Phillip H Jones.	9B_2: "Low-Power Reconfigurable Component Utilization in a High-Level Synthesis Flow", Dimitris Bekiaris, George Economakos, Efstathios Sotiriou-Xanthopoulos, Dimitrios Soudris.
	9A_3: "Design-For-Diversity for Improved Fault-Tolerance of TMR Systems on FPGAs", Rizwan A. Ashraf, Ouns Mouri, Rami Jadaa, Ronald F. DeMara.	9B_3: "RAP: More Efficient Memory Access in Highly Speculative Execution on Reconfigurable Adaptive Computers", Benjamin Thielmann, Thorsten Wink, Jens Huthmann, Andreas Koch.
	9A_4: "An Architecture for Reconfigurable Multi-core Explorations", Olivier Serres, Vikram K. Narayana, Tarek El-Ghazawi.	
16:40 - 16:45	Closing	

Poster Session A	Poster Session B
PA_1: "Robustness analysis of different AES implementations on SRAM based FPGAs", Uli Kretzschmar, Armando Astarloa, Jesús Lázaro, Unai Bidarte, Jaime Jimenez.	PB_1: "Techniques for Dynamically Mapping Computations to Coprocessors", João Carlos Viegas Marting Bispo, João M. P. Cardoso.
PA_2: "Efficient Dual-Rail Implementations in FPGA using Block RAMs", Shivam Bhasin, Sylvain Guilley, Youssef Souissi, Tarik Graba, Jean-Luc DANGER.	PB_2: "Rainbow - An OS Extension for Hardware Multitasking on Dynamically Partially Reconfigurable FPGAs", Krzysztof Jozwik, Hiroyuki Tomiyama, Masato Edahiro, Shinya Honda, Hiroaki Takada.
PA_3: "Versatile FPGA Architecture for Skein Hashing Algorithm", David M. Webster, Marcin Lukowiak.	PB_3: "Scalable Models for Autonomous Self-Assembled Reconfigurable Systems", Teresa G. Cervero, Sebastián López, Roberto Sarmiento, Tannous Frangieh, Peter Athanas.
PA_4: "GPU vs FPGA: Example Application on White Light Interferometry", Alexander Pacholik, Marcus Müller, Wolfgang Fengler, Torsten Machleidt, Karl-Heinz Franke.	PB_4: "LiSARD: LabVIEW Integrated Softcore Architecture for Reconfigurable Devices", Alexander Pacholik, Johannes Klöckner, Marcus Müller, Irina Gushchina, Wolfgang Fengler.
PA_5: "Spectral Method Characterization on FPGA and GPU Accelerators",Karl Savio Pimenta Pereira, Peter Athanas,Heshan Lin,Wu Feng.	PB_5: "EDA Environment for Evaluating a New Switch-Block-Free Reconfigurable Architecture", Masatoshi Nakamura, Masato Inagi, Kazuya Tanigawa, Tetsuo Hironaka, Masayuki Sato, Takashi Ishiguro.

Poster Session C	Poster Session D
PC_1: "Fixed-Point CORDIC-Based QR Decomposition by Givens Rotations on FPGA", Dongdong CHEN, Mihai SIMA.	PD_1: "A Coarse-Grained Reconfigurable Processor for Sequencing and Phylogenetic Algorithms in Bioinformatics", Pei Liu, Fatemeh Ostad Ebrahim, Kolin Paul, Ahmed Hemani.
PC_2: "Analysis of Parallel Sorting Algorithms in K-best Sphere-Decoder Architectures for MIMO Systems", Pedro Cervantes-Lozano, Luis Fernando González-Pérez, Andrés David García-García.	PD_2: "Reconfigurable Block Floating Point Processing Elements in Virtex Platforms", Guillermo Conde, Gregory W. Donohoe.
PC_3: "Design and Implementation of a simplified Turbo Decoder for 3GPP2", Lennin Conrado Yllescas-Calderón, Joaquin Adrian Espino-Orozco, Ramon Parra-Michel, Luis Fernando González-Pérez.	PD_3: "Digital Talking Book Player for the Visually Impaired Using FPGAs", Azadeh Nazemi, Cesar Ortega-Sanchez, Iain Murray.
PC_4: "Arbitrary Distribution Random Variable Generator for Channel Emulators", Rosalba del Refugio Zarate Martinez, Fernando Peña Campos, Javier Vazquez Castillo.	PD_4: "Using Self-Reconfiguration to Increase Manufacturing Yield of CNTFET-Based Architectures Hui Zhu; Sébastien Le Beux; Nataliya Yakymets; Ian O'Connor.
PC_5: "Performance-Area Improvement by Partial Reconfiguration for an Aerospace Remote Sensing Application", Luis Andres Cardona, Jharna Agrawal, Yi Guo, Joan Oliver, Carles Ferrer.	PD_5: "Hardware OS Communication Service and Dynamic Memory Management for RSoCs Surya Narayanan , Daniel Chillet, Sebastien Pillement , Ioannis Sourdis.
PC_6: "Reconfigurable FPGA-Based Unit for Singular Value Decomposition of Large m x n Matrices", Luis M. Ledesma-Carrillo, Eduardo Cabal-Yepez, Rene de J. Romero-Troncoso, Arturo Garcia-Perez, Roque A. Osornio-Rios, Tobia D. Carozzi.	PD_6: "Dynamic processor reconfiguration", M. Hübner, C. Tradowsky, D. Göhringer, L. Braun, F. Thoma, J. Henkel, J. Becker.

Poster Session E	Poster Session F
PE_1: "GIMME - A General Image Multiview Manipulation Engine", Carl Ahlberg, Jörgen Lidholm, Fredrik Ekstrand, Giacomo Spampinato, Mikael Ekström, Lars Asplund.	PF_1: "Toward all optical interconnections in chip Multiprocessor", Malek Channoufi, Pierre Lecoy, Rabah Attia, Bruno Delacressoniere.
PE_2: "Low-Cost TMR for Fault-Tolerance on Coarse-Grained Reconfigurable Architectures", Thomas Schweizer, Philipp Schlicker, Sven Eisenhardt, Tommy Kuhn, Wolfgang Rosenstiel.	PF_2: "Network on Chip Architectures for High Performance Digital Signal Processing Using a Configurable Core", Juan Carlos Pena Ramos, Ramon Parra Michel.
PE_3: "A PID Controller Applied to the Gain Control of a CMOS Camera Using Reconfigurable Computing", Drausio Linardi Rossi, João Miguel Gago Pontes de Brito Lima, Vanderlei Bonato, Eduardo Marques.	PF_3: "Enhancing the Randomness of a Combined True Random Number Generator Based on the Ring Oscillator Sampling Method", Mieczyslaw Jessa, Lukasz Matuszewski.
PE_4: "FPGA Based Acceleration of Decimal Operations", Alberto Nannarelli.	PF_4: "RAM-Based Ultra-Lightweight FPGA Implementation of PRESENT", Elif Bilge Kavun, Tolga Yalcin.
PE_5: "MiniMIPS: An 8-Bit MIPS in an FPGA for Educational Purposes", Cesar Ortega-Sanchez.	PF_5: "Fault Tolerance Analysis and Self-Healing Strategy of Autonomous, Evolvable Hardware Systems", Ruben Salvador, Andres Otero, Javier Mora, Eduardo de la Torre, Lukáš Sekanina, Teresa Riesgo.
PE_5: "Linking Formal Description and Simulation of Runtime Reconfigurable Systems", Thilo Pionteck, Christoph Osterloh, Carsten Albrecht.	