2009 International Conference on Reconfigurable Computing and FPGAs, ReConFig09
Preliminary Program

Wednesday 9 December

8:00 - 19:00 Registration

8:45-9:00 Opening

9:00-10:00 Keynote 1: Taming Programmable Concurrency, Patrick Lysaght, Senior Director, Xilinx Research Labs

10:00-10:15 Short Break

10:15-11:30

Parallel General Session : GS1 -Arithmetics

GS1_1 : FPGA Implementation of a Decimal Floating-Point Accurate Scalar Product Unit with a Parallel Fixed-Point Multiplier. *Malte Baesler and Thomas Teufel. (119)*

GS1_2 : Decimal adder/subtractors in FPGA: Eficient 6-input LUT implementations. *Martín Vázquez, Gustavo Sutter, Gery Bioul and Jean Pierre Deschamps. (68)*

GS1_3 : A FPGA IEEE-754-2008 DECIMAL64 FLOATING-POINT MULTIPLIER. *Carlos Minchola and Gustavo Sutter. (80)*

Parallel General Session : GS2 -Run Time Application

GS3_1 : Runtime memory allocation in a heterogeneous reconfigurable platform. *Vlad-Mihai Sima and Koen Bertels. (106)*

GS3_2 : Hotspot Mitigation using Dynamic Partial Reconfiguration for Improved Performance. *Adwait Gupte and Phillip Jones. (133)*

GS3_3 : A systolic array based architecture for implementing multivariate polynomial interpolation tasks. *Rafael Arce, Edusmildo Orozco and Dorothy Bollman.(48)*

11:30-12:00 Coffee Break

12:00-13:00 **General Session : GS3 - New FPGA Architectures**

GS2_1 : A Novel High-Density Single-Event Upset Hardened Configurable SRAM Applied to FPGA. Lei Wang, Lei Chen, Zhiping Wen, Huabo Sun and Shuo Wang. (35)

GS2_2 : MRAM based eFPGAs: programming and silicon flows, exploration environments, MRAM current state in Industry and its unique potentials for FPGAs. Yoann Guillemenet, Syed Zahid Ahmed, Lionel Torres, Alexandre Martheley, Julien Eydoux, Laurent Rougé, Jean-Baptiste Cuelle and Gilles Sassatelli. (57)

GS2_3 : A New CLB Architecture for Tolerating SEU in RAM-based FPGAs, Alireza Rohani, Hamid R. Zarandi (97)

13:00-15:00 LUNCH

15:00-16:40 **Session HPC1 : Track on High Performance Reconfigurable Computing**

HPC1_1: A Traversal Cache Framework for FPGA Acceleration of Pointer Data Structures: A Case Study on Barnes-Hut N-body Simulation. *James Coole, John Wernsing and Greg Stitt (120)*

HPC1_2: Triple Line-based Playout for Go --- An Accelerator of Monte Carlo Go. *Kenichi Koizumi, Mary Inaba, Kei Hiraki, Yasuo Ishii, Takefumi Miyoshi and Kazuki Yoshizoe (51)*

HPC1_3: Scalability Studies of the BLASTn Scan and Ungapped Extension Functions. *Siddhartha Datta and Ron Sass (32).*
HPC1_4: Low Power, Reconfigurable Computing Platform for Spacecraft. *Guillermo Conde, Greg Donohoe and Siva Maheswaran. (125)*

16:40-17:00 Introduction to Poster session 1 (8 posters general sessions)
17:00-17:30 Coffee Break & Poster session 1
17:30-19:10 **Sassion BSA: Track Bio Inspired and Self Adaptive Computing**

BSA1_1 : Effects of Simplistic Online Synthesis for AMIDAR Processors. *Stefan Döbrich and Christian Hochberger. (72)*

BSA1_2 : Implementation of a Dynamic Fault-Tolerance Scaling Technique on a Self-adaptive Hardware Architecture. *Javier Soto, Juan Manuel Moreno, Jordi Madrenas and Joan Cabestany. (45)*

BSA1_3 : Bio-Inspired Self-Testing and Self-Organizing Bit Slice Processors. *ANDRE STAUFFER and JOEL ROSSIER. (7)*

BSA1_4 : A Reconfigurable Design Framework for FPGA Adaptive Computing. *Ming Liu, Zhonghai Lu, Wolfgang Kuehn, Shuo Yang and Axel Jantsch.(105)*

Thursday 10 December

8:30 - 19:00 Registration

8:45-9:40 Keynote 2: Adaptivity, Reliability and Performance in future SoCs - Multi-Core dynamically reconfigurable Architectures in the Nano Era - Jürgen Becker, Karlsruhe Institute of Technology - KIT, Germany
9:40-9:45 Short Break
9:45-10:35 **Session DSP1 : session on Reconfigurable Computing for DSP and Communications**

DSP1_1: Enhancing the Productivity of Radio Designers with RapidRadio. *Jorge Suris Pietri, Adolfo Recio and Peter Athanas.(66)*

DSP1_2: Design And Implementation of a Configurable Interleaver/Deinterleaver for Turbo Codes in 3GPP Standard. *Hector Borrayo, Ramon Parra, Luis González and Claudia Feregrino (99)*

10:35-11:00 Introduction to Poster session 2 (1 poster BSA + 4 posters DSP + 3 posters MPSOC
11:00-11:30 Coffee Break & Poster Session 2

11:30-13:10

Session HPC2 : Track on High Performance Computing	**Session MPSOC1 : Track Multiprocessor Systems and Networks on Chip**
HPC2_1: A scalable architecture for multivariate polynomial evaluation on FPGA. *Mathieu Allard, Patrick Grogan and Jean-Pierre David (62).*	MPSOC1_1: Self-Adaptive Network Interface (SANI): local component of a NoC configuration manager. *Rachid DAFALI and Jean-Philippe Diguet (115)*
HPC2_2: Communication Performance Characterization for Reconfigurable Accelerator Design on the XD1000. *Tobias Schumacher, Tim Süß, Christian Plessl and Marco Platzner (63).*	MPSOC1_2: A Framework for 2.5D NoC Exploration using Homogeneous Networks over Heterogeneous Floorplans. *Vitor de Paulo and Cristinel Ababei (19)*

HPC2_3: FPGA-based Online Induction Motor Multiple-fault Detection with Fused FFT and Wavelet Analysis. *Roque Osornio-Rios, Eduardo Cabal-Yepez, Rene Romero-Troncoso, Jose Razo-Hernandez and Ricardo Lopez-Garcia (56).*

MPSOC1_3: Overview of FPGA-Based Multiprocessor Systems. *Taho Dorta, Jaime Jiménez, José Luis Martín, Unai Bidarte and Armando Astarloa. (28)*

HPC2_4: A Modular Approach to Heterogeneous Biochemical Model Simulation on an FPGA. *Hideki Yamada, Yasunori Osana, Tomoya Ishimori, Tomonori Ooya, Masato Yoshimi, Yuri Nishikawa, Akira Funahashi, Noriko Hiroi, Hideharu Amano, Yuichiro Shibata and Kiyoshi Oguri (116).*

MPSOC1_4: A Fault-Tolerant Layer for Dynamically Reconfigurable Multi-Processor System-on-Chip. *Hung-Manh Pham, Sebastien Pillement and Didier Demigny. (29)*

13:10-15:00 LUNCH

15:00-16:15 **Session DSP2 : session on Reconfigurable Computing for DSP and Communications**

DSP2_1: Design of Coarse-Grained Dynamically Reconfigurable Architecture for DSP Applications. *Chenxin Zhang, Thomas Lenart, Henrik Svensson and Viktor Öwal (26)*

DSP2_2: High Efficiency Space-Based Software Radio Architectures: A Minimum Size, Weight, and Power TeraOps Processor. *Mark E, Dunham, Zachary K. Baker, Matthew Stettler, Michael Pigue, Paul Graham, Eric Schmierer and John Power (117)*

DSP2_3: A Dynamically Reconfigurable Platform for Fixed-Point FIR Filters. *Daniel Llamocca, Marios Pattichis and Alonzo Vera (131).*

16:15-16:40 Introduction to Poster session 3 (3 posters RT + 6 posters HPRC)

16:40-17:10 Coffee Break & Poster Session 3

17:10-18:50 **Session RT : Track on Reconfiguration Techniques**

RT1 : Virtualization of Computing Resources in RCS for Multi-Task Stream Applications. *Lev Kirischian, Victor Dumitriu and Peter Chun. (82)*

RT2 : Runtime Temporal Partition Assembly to Reduce FPGA Reconfiguration Time. *Abelardo Jara-Berrocal and Ann Gordon-Ross. (64)*

RT3 : Design and Performance of a Grid of Asynchronously Clocked Run-Time Reconfigurable Modules on a FPGA. *Jochen Strunk, Toni Volkmer, Wolfgang Rehm and Heiko Schick. (87)*

20:00 - 22:00 Conference Dinner

Friday 11 December

8:30 - 12:00 Registration

9:00-10:15 **Session RR : Track on Reconfigurable computing for Robotics**

RR1: A reconfigurable architecture for stereo-assisted detection of point-features for robot mapping.*John Kalomiros and John Lygouras (11).*

RR2: FPGA Implementation for Direct Kinematics of a Spherical Robot Manipulator.*Diego F. Sánchez, Daniel M. Muñoz, Carlos H. Llanos and José M. Motta (65)*

RR3: Parallax-Docking and Reconfiguration of Field Programmable Robot Arrays using an Intermittently-Powered One-Hot Controller.*Mark Arnold and Jung Cho (109)*

10:15-10:25 Short break

10:25-11:40 **Session SC1 : Track on Reconfigurable Computing for Security and Cryptography**

SC1_1: Improving the Security of Dual Rail Logic in FPGA using Controlled Placement and Routing.*emna amouri, Zied Marrakchi, Hayder Mrabet and Habib Mehrez (18)*

SC1_2: Accelerating Cryptographic Applications Using Dynamically Reconfigurable Functional Units.*Antoine Trouve, Lovic Gauthier, Takayuki Kando, Pradeep Rao, Benoit Ryder, Sebastien Pouzols, Norifumi Yoshimatsu and Kazuaki Murakami. (9)*

SC1_3: Tailoring a Reconfigurable Platform to SHA-256 and HMAC through Custom Instructions and Peripherals.*Marcio Juliato and Catherine Gebotys (60)*

11:40-12:00 Introduction to Poster Session 4 (8 posters SC + 2 posters RR)

12:00-12:25 Coffee Break & Poster Session 4

12:25-13:40 **Session SC2 : Track on Reconfigurable Computing for Security and Cryptography**

SC2_1: DPL on Stratix II FPGA: What to Expect ?*Laurent SAUVAGE, Maxime NASSAR, Sylvain GUILLEY, Florent FLAMENT, Jean-Luc DANGER and Yves MATHIEU(54).*

SC2_2: Observing the randomness in RO-based TRNG.*Nathalie BOCHARD, Florent BERNARD and Viktor FISCHER (31)*

SC2_3: Proof-carrying Hardware: Towards Runtime Verification of Reconfigurable Modules.*Stephanie Drzevitzky, Uwe Kastens and Marco Platzner. (95)*

13:40-13:45 Closing

Poster Session 1

Prevention of Hot Spot Development on Coarse-Grained Dynamically Reconfigurable Architectures. Sven Eisenhardt, Thomas Schweizer, Andreas Bernauer, Tommy Kuhn, Wolfgang Rosenstiel

Floating Point Hardware for Embedded Processors in FPGAs: Design Space Exploration for Performance and Area. Taciano A. Rodolfo, Ney L. V. Calazans, Fernando G. Moraes

A 10 Gbps OTN Framer Implementation Targeting FPGA Devices. Guilherme Guindani, Frederico Ferlini, Jeferson Oliveira, Ney Calazans, Daniel Pigatto, Fernando Moraes

FPGA IMPLEMENTATIONS OF BCD MULTIPLIERS. Gustavo Sutter, Elías Todorovich, Gery Bioul, Martín Vazquez, J-P. Deschamps

Matrix Multiplication based on Scalable Macro-Pipelined FPGA Accelerator Architecture. Jiang Jiang, Vincent Mirian, Kam Pui Tang, Paul Chow, Zuocheng Xing

PCIREX: A Fast Prototyping Platform for TMR Dynamically Reconfigurable Systems. Armando Astarloa, Jesús Lázaro, Unai Bidarte, Aitzol Zuloaga, Jaime Jiménez

Speeding up Fault Injection for Asynchronous Logic by FPGA-based Emulation. Marcus Jeitler, Jakob Lechner

Base-Calling in DNA Pyrosequencing with Reconfigurable Bayesian Network. Mingjie Lin, Yaling Ma

Poster Session 2

FPGA Implementation of Izhikevich Spiking Neural Networks for Character Recognition. Kenneth L. Rice, Mohammad A. Bhuiyan, Tarek M. Taha, Christopher N. Vutsinas, Melissa C. Smith

Efficient PGA LFSR Implementation Whitens Pseudorandom Numbers. Leonard Colavito, Dennis Silage

Composite Look-Up Table Gaussian Pseudo-Random Number Generator. Leonard Colavito, Dennis Silage

A New Approach to Implement Discrete Wavelet Transform using Collaboration of Reconfigurable Elements. Asadollah Shahbahrami, Mahmood Ahmadi, Stephan Wong, Koen Bertels

Signal Processing Domain Application Mapping On The Brick Reconfigurable. Juan Fernando Eusse Giraldo, Ricardo Pezzuol Jacobi

Symmetric multiprocessor systems on FPGA. Pablo Huerta, Javier Castillo, Cesar Pedraza, Javier Cano, Jose Ignacio Martinez

Modeling and Analyzing of Blocking Time Effects on Power Consumption in Network-on-Chips. Arghavan Asad, Amir Ehsani Zonouz, Mehrdad Seyrafi, Mohsen Soryani, Mahmood Fathy

High-level FPGA Programming through Mapping Process Networks to FPGA Resources. Fritz Mayer-Lindenberg

Poster Session 3

Multiprocessor Task Migration Implementation in a Reconfigurable Platform. Laurent Gantel, Salah Layouni, Mohamed El Amine Benkhelifa, François Verdier, Stéphanie Chauvet

Composable And Persistent-State Application Swapping On FPGAs Using Hardwired Network on Chip. Muhammad Aqeel Wahlah, Kees Goossens

New OPBHWICAP interface for realtime Partial reconfiguration of FPGA. Julien Delorme, Amor Nafkha, Pierre Leray, Christophe Moy

An FPGA-based custom high performance interconnection network. Mondrian Nüssle, Benjamin Geib, Holger Fröning, Ulrich Brüning

Low Power RTL Exploration Mechanism based on the Cache Parameters. Abel Guilhermino Silva-Filho, Sidney Marlon Lopes de Lima, Frederico Cox Cavalcancti Lins Junior

Hardware Accelerator for Full-Text Search (HAFTS) with Succinct Data Structure. Naoki Tanida, Takeshi Yoshino, Mary Inaba, Kei Hiraki

Acceleration of Fractal Image Compression Using the Hardware-Software Co-Design Methodology. Oscar Alvarado Nava, Arturo Díaz Pérez

FPGA Implementation of the Generalized Hough Transform. Sergio Rubén Geninatti, José Ignacio Benavides Benítez, Manuel Hernández Calviño, Nicolás Guil Mata, Juan Gómez Luna

An Optimized System for Multiple Sequence Alignment. Caglar Yilmaz, Mustafa Gok

Poster Session 4

Protecting the NOEKEON Cipher Against SCARE Attacks in FPGAs by using Dynamic Implementations. Julien Bringer, Herve Chabanne, Jean-Luc Danger

Implementing a Protected Zone in a Reconfigurable Processor for Isolated Execution of Cryptographic Algorithms. A. Onur Durahim, Erkay Savas, Kazim Yumbul

Combined SCA and DFA Countermeasures Integrable in a FPGA Design Flow. Shivam BHASIN, Jean-Luc DANGER, Florent FLAMENT, Tarik GRABA, Sylvain GUILLEY, Yves MATHIEU, Maxime NASSAR, Laurent SAUVAGE, Nidhal SELMANE

Efficient Technique for the FPGA Implementation of the AES MixColumns Transformation. Solmaz Ghaznavi, Catherine Gebotys, Reouven Elbaz

Lightweight Cryptography for FPGAs. Panasayya Yalla, Jens-Peter Kaps

FPGA Implementation of an Elliptic Curve Processor using the GLV Method. Mark Hamilton, William P. Marnane

Reconfigurable Hardware Implementation of Arithmetic Modulo Minimal Redundancy Cyclotomic Primes for ECC. Brian Baldwin, William P Marnane, Robert Granger

Realizing Arbitrary-Precision Modular Multiplication with a Fixed-Precision Multiplier Datapath. Johann Großschädl, Erkay Savas, Kazim Yumbul

Fuzzy Control for Cyclist Robot Stability using FPGAs. Yesid Enrique Castro Caicedo, Carlos Humberto Llanos Quintero, Walter de Britto Vidal Filho, Leandro dos Santos Coelho

On the implementation of central pattern generators for periodic rhythmic locomotion. Cesar Torres-Huitzil