ReConFig´08 - Program

Wednesday 3 December	
8:00-17:00	Registration
8:45-9:00	Opening
9:00-9:55	Keynote
9:55-10:00	Short break
10:00-11:15	Parallel General Sessions: GS1 – Applications I and GS2 - Processors
11:15-11:40	Coffee break
11:40-13:20	Parallel General Sessions: GS3 - Applications II and GS4 - Reconfigurability
13:20-15:00	Lunch
15:00-16:30	General Session GS5 – Processors II Introduction to poster session 1
16:30-17:10	Coffee break - Poster session 1
17:10-18:50	General Session GS6 – Methodologies

Thursday 4 December	
8:00-17:00	Registration
8:30-9:10	Invited talk
9:10-9:15	Short break
9:15-11:00	Session BSA: Track on Bioinspired Reconfigurable Computing Systems and Self-adaptive Computing Introduction to poster session 2
11:00-11:30	Coffee break - Poster session 2
11:30-13:35	Session HP: Track on High Performance Reconfigurable Computing
13:35-15:00	Lunch
15:00-16:40	Session DSP 1: Track on Reconfigurable Computing for DSP and Communications I Introduction to poster session 3
16:50-17:20	Coffee break - Poster session 3
17:20-19:00	Session DSP2: Track on Reconfigurable Computing for DSP and Communications II
20:00-22:00	Gala dinner by the beach

Friday 5 December	
8:30-11:30	Registration
9:00-9:30	Invited talk - TBC
9:30-9:40	Short break
9:40-11:30	Session SC1: Track on Reconfigurable Computing for Security and Cryptography I Introduction to poster session 4
11:30-12:00	Coffee break - Poster session 4
12:00-13:15	Session SC2:Track on Reconfigurable Computing for Security and Cryptography II
13:15-13:30	Closing and awards presentation
20:00-Until late	Social event at Mexican Cantina (Family Style Restaurant Bar)

ReConFig´08

2008 International Conference on ReConFigurable Computing and FPGAs

Cancún, México, December 3-5, 2008

	P4_1: Enhanced Correlation Power Analysis using Key Screening Techniques *Toshihiro Katashita, Akashi Satoh, Takeshi Sugawara, Naofumi Homma and Takafumi Aoki* P4_2: Enhancing an Embedded Processor Core with a Cryptographic Unit for Speed and Security *Ovunc Kocabas, Erkay Savas and Johann Groszschaedl* P4_3: Triple Rail Logic Robustness against DPA *Victor Lomne, Thomas Ordas, Philippe Maurine, Lionel Torres, Michel Robert, Rafael Soares and Ney Calazans* P4_4: FPGA Implementation and Performance Evaluation of AES-CCM Cores for Wireless Networks *Ignacio Algredo-Badillo, Claudia Feregrino, René Cumplido and Miguel Morales-Sandoval* P4_5: Power Consumption Estimations vs Measurements for FPGA-Based Security Cores *Dimitrios Meintanis and Ioannis Papaefstathiou* P4_6: High Performance Implementation of a Public Key Block Cipher - MQQ, for FPGA Platforms *Mohamed El-Hadedy, Danilo Gligoroski and Svein J. Knapskog* P4_7: Key Research Issues for Reconfigurable Network-on-Chip *R. Dafali, J.-Ph. Diguet, and M. Sevaux* P4_8: SoC-MPI: A Flexible Message Passing Library for Multiprocessor Systems-on-Chips *Philipp Mahr, Christian Lörchner, Harold Ishebabi and Christophe Bobda* P4_9: Design Space Exploration and Performance Analysis for the Modular Design of CVS in a Heterogeneous MPSoC *Z. Jian Jia, Tomás Bautista, Antonio Núnez, Cayetano Guerra, and Mario Hernández*
12:00-13:15	Session SC2:Track on Reconfigurable Computing for Security and Cryptography II
12:00-12:25 12:25-12:50	SC2_1: Celator: A Multi-algorithm Cryptographic Co-processor *Daniele Fronte, Annie Perez and Eric Payrat* SC2_2: A Reversible Data Hiding Algorithm for Radiological Medical Images and its Hardware Implementation *Z. Jezabel Guzmán Zavaleta, Claudia Feregrino Uribe, and René Cumplido*

ReConFig´08 - Program

Wednesday 3 December		
8:00-17:00	Registration	
8:45-9:00	Opening	
9:00-9:55	Keynote “High Throughput Network Infrastructure Functions on FPGAs” Viktor K Prasanna, University of Southern California	
9:55-10:00	Short break	
10:00-11:15	Parallel General Sessions: GS1 – Applications I and GS2 - Processors	
10:00-10:25	GS1_1: Reconfigurable PDA for the Visually Impaired Using FPGAs *Xuan Zhang, Cesar Ortega-Sánchez and Iain Murray*	GS2_1: Automatic Synthesis of Multiprocessor Systems from Parallel Programs under Preemptive Scheduling *Harold Ishebabi, Philipp Mahr and Christophe Bobda*
10:25-10:50	GS1_2: Embedded Harmonic Control for Trajectory Planning in Large Environments *César Torres-Huitzil, Bernard Girau, Amine Boumaza and Bruno Scherrer*	GS2_2: Design and Implementation of a Resource-Efficient Communication Architecture for Multiprocessors on FPGAs *Xiaofang Wang and Swetha Thota*
10:50-11:15	GS1_3: Flexible Architecture for Three Classes of Optical Flow Extraction Algorithms *José Hugo Barrón-Zambrano, César Torres-Huitzil and Mauricio Cerda*	GS2_3: Automatic Instruction-Set Extensions with the Linear Complexity Spiral Search *Carlo Galuzzi, Dimitris Theodoropoulos, Roel Meeuws, and Koen Bertels*
11:15-11:40	Coffee break	
11:40-13:20	Parallel General Sessions: GS3 - Applications II and GS4 - Reconfigurability	
11:40-12:05	GS3_1: A Real-Time Embedded System for Stereo Vision Preprocessing Using an FPGA *Anders Kjær-Nielsen, Lars Baunegaard With Jensen, Anders Stengaard Sørensen, and Norbert Krüger*	GS4_1: A Framework for the Exploration of RTOS Dedicated to the Management of Hardware Reconfigurable Resources *J.C. Prevotet, A. Benkhelifa, B. Granado, E. Huck, B. Miramond, F. Verdier, D. Chillet, and S. Pillement*
12:05-12:30	GS3_2: Finite Precision Analysis of the 3GPP Standard Turbo Decoder for Fixed-Point Implementation in FPGA Devices *Anabel Morales-Cortés, R. Parra-Michel, Luis F. González-Pérez, and Gabriela Cervantes T.*	GS4_2: Optimizing Partial Reconfiguration of Multi-context Architectures *Sven Eisenhardt, Tobias Oppold, Thomas Schweizer and Wolfgang Rosenstiel*
12:30-12:55	GS3_3: Parallel Processor for 3D Recovery from Optical Flow *José Hugo Barrón-Zambrano, Fernando Matín del Campo-Ramírez and Miguel Arias-Estrada*	GS4_3: Automatic Construction of Large-Scale Regular Expression Matching Engines on FPGA *Yi-Hua E. Yang and Viktor K. Prasanna*
12:55-13:20	GS3_4: A Reconfigurable Platform for Frequent Pattern Mining *Song Sun, Michael Steffen, and Joseph Zambreno*	GS4_4: A Hardware Task-Graph Scheduler for Reconfigurable Multi-tasking Systems *Juan Antonio Clemente, Carlos González, Javier Resano, and Daniel Mozos*
13:20-15:00	Lunch	

15:00-16:30	General Session GS5 – Processors II Introduction to poster session 1
15:00-15:25	GS5_1: Optimized Architectural Synthesis of Fixed-Point Datapaths *Gabriel Caffarena, Juan A. López, Gerardo Leyva, Carlos Carreras and Octavio Nieto-Taladriz*
15:25-15:50	GS5_2: Developing an MMX Extension for the Microblaze Soft Processor *Manuel Hernández Calviño, Sergio Rubén Geninatti and José Ignacio Benavides Benítez*
15:50-16:30	Short oral introduction to papers presented at poster session 1
16:30-17:10	Coffee break - Poster session 1
	P1_1: Loop Transformations to Reduce the Dynamic FPGA Reconfiguration Overhead *Tom Degryse, Karel Bruneel, Harald Devos and Dirk Stroobandt* P1_2: Arithmetic Operations and their Energy Consumption in the Nios II Embedded Processor *David M. Cambre and Elías Todorovich* P1_3: Leveraging Firmware in Multichip Systems to Maximize FPGA Resources: An Application of Self-Partial Reconfiguration *Juan Galindo, Eric Peskin, Brad Larson and Gene Roylance* P1_4: Operating System for Symmetric Multiprocessors on FPGA *Pablo Huerta, Javier Castillo, Carlos Sánchez, and Jose Ignacio Martínez* P1_5: Dynamically Reconfigurable Split Cache Architecture *Luiza M.N. Coutinho, Jose L.D. Mendes, and Carlos A.P.S. Martins* P1_6: Finite Domain Constraints Based Delay Aware Placement Tool for FPOAs *Rohit Saraswat and Brandon Eames* P1_7: Enhanced Methodology and Tools for Exploring Domain-Specific Coarse-grained FPGAs *Husain Parvez, Zied Marrakchi and Habib Mehrez* P1_8: Configurable-System-on-Programmable-Chip for Power Electronics Control Applications *Armando Astarloa, Unai Bidarte, Jesús Lázaro, Jon Andreu and José Luis Martín* P1_9: Integrating Logic Analyzer Functionality into VHDL Designs *G. Knittel, S. Mayer, and C. Rothlaender*
17:10-18:50	General Session GS6 – Methodologies
17:10-17:35	GS6_1: An ILP Formulation for the Task Graph Scheduling Problem Tailored to Bi-dimensional Reconfigurable Architectures *F. Redaelli, M.D. Santambrogio, and S. Ogrenci Memik*

Friday 5 December	
8:30-11:30	Registration
9:00-9:30	Invited talk
9:30-9:40	Short break
9:40-11:30	Session SC1: Track on Reconfigurable Computing for Security and Cryptography I Introduction to poster session 4
9:40-10:05	SC1_1:17 Analysis and Enhancement of Random Number Generator in FPGA Based on Oscillator Rings *Knut Wold and Chik How Tan*
10:05-10:30	SC1_2: Parametric, Secure and Compact Implementation of RSA on FPGA *Ersin Öksüzoglu and Erkay Savas*
10:30-10:55	SC1_3: FPGA Implementation of an Elliptic Curve Cryptosystem over GF(3^m) *Ilker Yavuz, Siddika Berna Örs Yalçin, and Çetin Kaya Koç*
10:55-11:30	Short oral introduction to papers presented at poster session 4
11:30-12:00	Coffee break - Poster session 4
	P4_1: Enhanced Correlation Power Analysis using Key Screening Techniques *Toshihiro Katashita, Akashi Satoh, Takeshi Sugawara, Naofumi Homma and Takafumi Aoki* P4_2: Enhancing an Embedded Processor Core with a Cryptographic Unit for Speed and Security *Ovunc Kocabas, Erkay Savas and Johann Groszschaedl* P4_3: Triple Rail Logic Robustness against DPA *Victor Lomne, Thomas Ordas, Philippe Maurine, Lionel Torres, Michel Robert, Rafael Soares and Ney Calazans* P4_4: FPGA Implementation and Performance Evaluation of AES-CCM Cores for Wireless Networks *Ignacio Algredo-Badillo, Claudia Feregrino, René Cumplido and Miguel Morales-Sandoval* P4_5: Power Consumption Estimations vs Measurements for FPGA-Based Security Cores *Dimitrios Meintanis and Ioannis Papaefstathiou* P4_6: High Performance Implementation of a Public Key Block Cipher - MQQ, for FPGA Platforms *Mohamed El-Hadedy, Danilo Gligoroski and Svein J. Knapskog*

18:10-18:35	DSP2_3: Universal Wavelet Kernel Implementation Using Reconfigurable Hardware *Christophe Desmouliers, Erdal Oruklu and Jafar Saniie*
18:35-19:00	DSP2_4: Design and Implementation of a Multi-standard Interleaver for 802.11a, 802.11n, 802.16e & DVB Standards *Carlos R. Sánchez-Ortiz, R. Parra-Michel, and M.E. Guzmán-Renteria*
20:00-22:00	Gala dinner by the beach

17:35-18:00	Architectural Model and Resource Estimation for Distributed Hardware Implementation of Discrete Signal Transforms *Rafael A. Arce-Nazario, Manuel Jiménez, and Domingo Rodríguez*
18:00-18:25	GS6_3: A Reconfiguration-aware Floorplacer for FPGAs *A. Montone, F. Redaelli, M.D. Santambrogio, and S. Ogrenci Memik*
18:25-18:50	GS6_4: The Effect of LUT and Cluster Size on a Tree Based FPGA Architecture *Umer Farooq, Zied Marrakchi, Hayder Mrabet and Habib Mehrez*

Thursday 4 December	
8:00-17:00	Registration
8:30-9:10	Invited talk "FPGA Design Future - and EETimes Survey" Craig Kief, FPGA Mission Assurance Center
9:10-9:15	Short break
9:15-11:00	Session BSA: Track on Bioinspired Reconfigurable Computing Systems and Self-adaptive Computing Introduction to poster session 2
9:15-9:40	BSA_1: Reconfigurability-Aware Structural Mapping for LUT-Based FPGAs *Karel Bruneel and Dirk Stroobandt*
9:40-10:05	BSA_2: Fast Implementation of a Bio-inspired Model for Decentralized Gathering *Bernard Girau and Cesar Torres-Huitzil*
10:05-10:30	BSA_3: Game-Theoretic Approach for Temperature-Aware Frequency Assignment with Task Synchronization on MP-SoC *Diego Puschini, Fabien Clermidy, Pascal Benoit, Gilles Sassatelli and Lionel Torres*
10:30-11:00	Short oral introduction to papers presented at poster session 2
11:00-11:30	Coffee break - Poster session 2
	P2_1: A Real-Time FPGA based Platform for Applications in Mechatronics *Roque A. Osornio-Rios, Rene de J. Romero-Troncoso, Luis Morales-Velazquez, J. Jesus de Santiago-Perez, Rooney de J. Rivera-Guillen, and J. de Jesus Rangel-Magdaleno* P2_2: Disparity Map Hardware Accelerator *Humberto Calderón, Jesús Ortiz, and Jean-Guy Fontaine* P2_3: A Novel Rekeying Message Authentication Procedure Based on Winternitz OTS and Reconfigurable Hardware Architectures *Abdulhadi Shoufan, Sorin A. Huss, Oliver Kelm and Sebastian Schipp* P2_4: Dynamic Self-Rescheduling of Tasks over a Heterogeneous Platform *Alécio P.D. Binotto, Edison P. Freitas, Marcelo Götz, Carlos E. Pereira, André Stork, and Tony Larsson*

	P2_5: A Hybrid FPGA/Coarse Parallel Processing Architecture for Multi modal Visual Feature Descriptors *Lars Baunegaard With Jensen, Anders Kjær Nielsen, Javier Díaz Alonso, Eduardo Ros, and Norbert Krüger* P2_6: A Temporal Partitioning Methodology for Reconfigurable High Performance Computers *Paulo S. Brandao do Nascimento, Victor W.C. de Medeiros, Viviane L.S. Souza, Abner C. Barros, and Manoel Eusebio de Lima* P2_7: Design and Implementation of Adaptive Viterbi Decoder For Using A Dynamic Reconfigurable Processor *Yuken Kishimoto, Shinichiro Haruyama and Hideharu Amano* P2_8: Power Consumption Reduction Explorations in Processors by Enhancing Performance Using Small ESL Reprogrammable eFPGAs *Syed Zahid Ahmed, Julien Eydoux, Michael Fernandez, Laurent Rougé, Gilles Sassatelli and Lionel Torres* P2_9: Parallel Backprojector for Cone-Beam Computer Tomography *Nikolay Sorokin*
	Session HP: Track on High Performance Reconfigurable Computing
	HP_1: Sequence Alignment with Traceback on Reconfigurable Hardware *Scott Lloyd and Quinn O. Snell* HP_2: A Message-Passing Hardware/Software Co-simulation Environment to Aid in Reconfigurable Computing Design using TMD-MPI *Manuel Saldaña, Emanuel Ramalho and Paul Chow* HP_3: FPGA Implementation of Pseudo Random Number Generators for Monte Carlo Methods in Quantitative Finance *Simon Banks, Philip Beadling and Andras Ferencz* HP_4: A Pthreads-Based MPI-1 Implementation for MMU-Less Machines *Juan A. Rico-Gallego, Jesus M. Alvarez-Llorente, Francisco J. Perogil-Duque, Pedro P. Antúnez-Gómez, and Juan C. Díaz-Martín* HP_5: A Hardware Filesystem Implementation for High-Speed Secondary Storage *Ashwin A. Mendon and Ron Sass*
	Lunch
	Session DSP 1: Track on Reconfigurable Computing for DSP and Communications I Introduction to poster session 3
	DSP1_1: Reconfigurable Cell Architecture for Systolic and Pipelined Computing Datapaths *Abdulrahaman Hanoun, Friedrich Mayer-Lindenberg and Bassel Soudan*

15:25-15:50	DSP1_2: Implementations and Optimizations of Pipeline FFTs on Xilinx FPGAs *Bin Zhou and David Hwang*
15:50-16:15	DSP1_3: Generalised Parallel Bilinear Interpolation Architecture for Vision Systems *Suhaib A. Fahmy*
16:15-16:50	Short oral introduction to papers presented at poster session 3
16:50-17:20	Coffee break - Poster session 3
	P3_1: A FFT/IFFT Design versus Altera and Xilinx Cores *C. Gonzalez-Concejero, V. Rodellar, A. Alvarez-Marquina, E. Martinez de Icaya, and P. Gomez-Vilda* P3_2: Using a CSP Based Programming Model for Reconfigurable Processor Arrays *Zain-ul-Abdin and Bertil Svensson* P3_3: A Novel FPGA Implementation of a Wideband Sonar System for Target Motion Estimation *Sheng Cheng, Chien-Hsun Tseng and Marina Cole* P3_4: Hybrid Architecture for Data-Dependent Superimposed Training in Digital Receivers *Fernando Martin del Campo, Rene Cumplido, Roberto Pérez-Andrade and A. G. Orozco-Lugo* P3_5: Part-E—A Tool for Reconfigurable System Design *Elmar Weber, Florian Dittmann and Norma Montealegre* P3_6: VIS2SOUND on Reconfigurable Hardware *C. Morillas, J.P. Cobos, F.J. Pelayo, A. Prieto, and S. Romero* P3_7: A Fast Emulation-Based NoC Prototyping Framework *Yana E. Krasteva, Francisco Criado, Eduardo de la Torre and Teresa Riesgo* P3_8: Power-Efficient High Throughput Reconfigurable Data path Design for Portable Multimedia Devices *Sohan Purohit, Sai Rahul Chalamalasetti, Martin Margala, and Pasquale Corsonello*
17:20-19:00	Session DSP2: Track on Reconfigurable Computing for DSP and Communications II
17:20-17:45	DSP2_1: A Comparison of Approaches for High-level Power Estimation of LUT-Based DSP Components *Ruzica Jevtic, Carlos Carreras, Domenik Helms and Gabriel Caffarena*
17:45-18:10	DSP2_2: FPGA Implementation of a Modulated Complex Lapped Transform for Watermarking Systems *Jose Juan Garcia-Hernandez, Claudia Feregrino-Uribe and Rene Cumplido*