

# ReConFig 06 PROGRAM

Wednesday, September 20th

8:00 - 9:00	Conference registration
9:00 - 10:00	ENC and ReConFig officinal opening
10:00 - 11:00	Keynote speech: Experience Sacaling Agile Devel, Dr. David Thomas, Bedarra Research, Canada (Shared with ENC 06)
11:10 – 13:10	<b>Session I: Reconfigurable Architectures I</b>
11:10 – 11:30	1. Javier Castillo Villar, Pablo Huerta Pellitero, Cesar Pedraza Bonilla and Jose Ignacio Martinez Torre. <i>A Self-reconfigurable Multimedia Placer on FPGA</i>
11:30 – 11:50	2. Marcelo Götz and Florian Dittmann. <i>Reconfigurable Microkernel-based RTOS: Mechanisms and Methods for Run-Time Reconfiguration</i>
11:50 – 12:10	3. Ricardo Ferreira, Marcos Vinicius Silva, Alisson Garcia and João Cardoso. <i>Mesh Mapping Exploration on Coarse Grained Reconfigurable Array Architectures</i>
12:10 – 12:30	4. Jacob Bower, David Thomas, Wayne Luk and Oskar Mencer. <i>A Reconfigurable Simulation Framework for Financial Computation</i>
12:30 – 12:50	5. Andres Cicuttin, Maria Liz Crespo, Alexander Shapiro and Nizar Abdallah. <i>A Block-Based Open Source Approach for a Reconfigurable Virtual Instrumentation Platform Using FPGA Technology</i>
12:50 – 13:10	6. Sumanta CHAUDHURI, Jean-Luc DANGER and Sylvain GUILLEY. <i>FASE: An Open Run-Time Reconfigurable FPGA Architecture for Tamper-Resistant and Secure Embedded Systems</i>
13:10 – 14:30	<b>LUNCH</b>
14:30 – 16:10	<b>Session II: Tools</b>
14:30 – 14:50	1. Samahi Abdelhalim, Bourennane el-bay and Boukhechem Sami. <i>Communications Interfaces Generation for HW/SW Architecture in the STARSoC Environment</i>
14:50 – 15:10	2. Jorge Silva and Eduardo Marques. <i>Executing Algorithms for Dynamic Dataflow Reconfigurable Hardware – The Operators Protocol</i>
15:10 – 15:30	3. Julio Oliveira, Thomas Schweizer, Tobias Oppold, Tommy Kuhn and Wolfgang Rosenstiel. <i>Tuning Coarse-Grained Reconfigurable Architectures towards an Application Domain</i>
15:30 – 15:50	4. Jorge Suris and Peter Athanas. <i>Exploring Non-Traditional Hardware-Software Interaction</i>
15:50 – 16:10	5. Heng Tan and Ronald DeMara. <i>A Physical Resource Management Approach to Minimizing FPGA Partial Reconfiguration Overhead</i>
16:10 – 16:30	<b>Coffee break</b>
16:30 – 18:10	<b>Session III: Applications I: Bio-inspired systems</b>
16:30 -16:50	1. Nilton Armstrong Jr., Heitor Lopes and Carlos Erig Lima. <i>Preliminary Steps Towards Protein Folding Prediction Using Reconfigurable Computing</i>
16:50 -17:10	2. Guilherme Moritz, Cristiano Jory, Heitor Lopes and Carlos Erig Lima. <i>Implementation of a Parallel Algorithm for Protein Pairwise Alignment Using Reconfigurable Computing</i>
17:10 -17:30	3. Rashad Oreifej, Carthik A Sharma and Ronald DeMara. <i>Expediting GA-Based Evolution Using Group Testing Techniques for Reconfigurable Hardware</i>
17:30 -17:50	4. Jorge Peña, Andrés Valencia and Mauricio Vanegas. <i>Digital Hardware Architectures of Kohonen's Self Organizing Feature Maps with Exponential Neighboring Function</i>
17:50 -18:10	5. Andres David García García, Carlos E. Gutierrez Salmerón and Reynaldo Félix. <i>Bio-inspired &amp; Traditional Approaches to obtain Fault Tolerance</i>
18:10 – 18:30	<b>Coffee break</b>
18:30 -19:30	Keynote speech: An Adaptive Packed-Mem Array, Michael Bender, State University of New York (Shared with ENC 06)

# ReConFig 06 PROGRAM

Thursday, September 21st

<b>8:00 – 9:00</b>	<b>Conference registration</b>
	<b>Session IV: Physical design</b>
10:00 -10:20	1. Timothy Lantz and Eric Peskin. <i>A QCA Implementation of a Configurable Logic Block for an FPGA</i>
10:20 -10:40	2. Ameet Chavan, Eric MacDonald, Gaurav Dukle and Ben Graniello. <i>Robust Ultra-Low Power Subthreshold Logic Flip-Flop Design for Reconfigurable Architectures</i>
10:40 -11:00	3. Marcos Rubén de Alba Rosano and Andres David García García. <i>Measuring Leakage Power in Nanometer CMOS 6T-SRAM Cells</i>
<b>11:00 – 11:10</b>	<b>Coffee break</b>
<b>11:10 – 13:10</b>	<b>Session V: Applications II</b>
11:10 – 11:30	1. Maurice Keller, Robert Ronan, William Marnane and Colin Murphy. <i>A <math>GF(2^{4m})</math> Inverter and its Application in a Tate Pairing Processor</i>
11:30 – 11:50	2. Ahmed Elhossini, Shawki Areibi and Robert Dony. <i>An FPGA Implementation of the LMS Adaptive Filter for Audio Processing</i>
11:50 – 12:10	3. Miguel Morales-Sandoval and Claudia Feregrino-Uribe. <i><math>GF(2^m)</math> Arithmetic Modules for Elliptic Curve Cryptography</i>
12:10 – 12:30	4. Elvira Martínez de Icaya, Victoria Rodellar, Coral González , Virginia Peinado and Vicente Garcia. <i>Design Space Exploration for an Adaptive Noise Cancellation Algorithm</i>
12:30 – 12:50	5. Santos Martin López Estrada and René Cumplido. <i>Decision Tree Based FPGA-Architecture for Texture Sea State Classification</i>
12:50 – 13:10	6. Hiroyuki Kawai, Yoshiki Yamaguchi and Moritoshi Yasunaga. <i>Realization of the sound space environment for the radiation-tolerant space craft</i>
<b>13:10 – 14:30</b>	<b>LUNCH</b>
<b>14:30 – 16:10</b>	<b>Session VI: Image and Video Processing</b>
14:30 – 14:50	1. S. L. Bishop, S. Rai, B. Gunturk, J. L. Trahan, and R. Vaidyanathan. <i>Reconfigurable Implementation of Wavelets Integer Lifting Transforms for Image Compression</i>
14:50 – 15:10	2. Griselda Saldaña and Miguel Arias. <i>Real Time FPGA-based Architecture for Video Applications</i>
15:10 – 15:30	3. José Martínez and Leopoldo Altamirano. <i>FPGA-based Pipeline Architecture to Transform Cartesian Images into Foveal Images by Using a new Foveation Approach</i>
15:30 – 15:50	4. Julio Cesar Sosa, Rocío Gómez-Fabela, José Antonio Boluda and Fernando Pardo. <i>Change-Driven Image Processing Architecture with Adaptive Threshold for Optical-Flow Computation</i>
15:50 – 16:10	5. Pedro Gomez, Francisco Diaz, Bogdan Belean, Raul Maultan, Benjamin Stetter, Rafael Martínez and Victoria Rodellar. <i>Robust cDNA microarray image processing on a hand-held device</i>
<b>16:10 – 16:30</b>	<b>Coffee break</b>
<b>16:30 – 18:10</b>	<b>Session VII: Reconfigurable Architectures II</b>
16:30 -16:50	1. Thorsten von Sydow, Matthias Korb, Bernd Neumann, Holger Blume and Tobias Noll. <i>Modelling and Quantitative Analysis of Coupling Mechanism of Programmable Processor Cores and Arithmetic Oriented EEFPGA Macros</i>
16:50 -17:10	2. Achim Rettberg, Florian Dittmann and Raphael Weber. <i>Towards the Implementation of Path Concepts for a Reconfigurable Bit-Serial Synchronous Architecture</i>
17:10 -17:30	3. Manuel Alejandro Saldaña De Fuentes, Daniel Nunes, Emanuel Ramalho and Paul Chow. <i>Configuration and Programming of Heterogeneous Multiprocessors on a Multi-FPGA System Using TMD-MPI</i>
17:30 -17:50	4. Mazen Saghier, Mohamad El-Majzoub and Patrick Akl. <i>Datapath and ISA Customization for Soft VLIW Processors</i>
17:50 -18:10	5. Daniel Mauricio Muñoz, Carlos Llanos, Mauricio Ayala-Rincón and Rudi H. van Els. <i>Implementation, Simulation and Validation of Dispatching Algorithms for Elevator Systems</i>
<b>18:10 – 18:30</b>	<b>Coffee break</b>
<b>18:30 -19:30</b>	<b>Keynote speech: Spectral Algorithms and Repr. Santosh Vampala, Math. Dept. MIT (Shared with ENC 06)</b>

# ReConFig 06 PROGRAM

Friday, September 22nd

8:00 – 9:00	Conference registration
9:00 – 10:00	Keynote speech: TBA, David Karchmer, Altera
10:00 – 10:10	Coffee break
10:10 -12:10	<b>Session VIII: Education and Applications</b>
10:10 -10:30	1. René de Jesús Romero-Troncoso, Arturo Garcia Perez, Jose Alberto Vite-Frias and Alejandro Ordaz. <i>8-bit CISC Microprocessor Core for Teaching Applications in the Digital Systems Laboratory</i>
10:30 -10:50	2. Gerardo Eli Martinez-Torres, Jose Martin Luna-Rivera and Raul Eduardo Balderas-Navarro. <i>A Versatile FPGA-Based Educational Platform for Wireless Transmission Using System Generator</i>
10:50 -11:10	3. Omar Piña-Ramirez, Raquel Valdes and Oscar Yáñez. <i>An FPGA Implementation of Linear Kernel Support Vector Machines</i>
11:10 -11:30	4. Julio Pimentel. <i>Implementation of Simulation Algorithms in FPGA for Real Time Simulation of Electrical Networks with Power Electronics Devices</i>
11:30 -11:50	5. Yogindra Abhyankar, Sajish C, Yogesh Agarwal and Subrahmanya C.R. <i>High Performance Power Spectrum Analysis Using a FPGA Based Reconfigurable Computing Platform</i>
11:50 -12:10	6. Ulises Silverio Mendoza-Camarena and René de Jesús Romero-Troncoso. <i>VHDL Core for the Computation of the One-Dimensional Discrete Cosine</i>
12:10 – 12:30	Coffee break
12:30 – 13:30	Keynote speech: Evolutionary Computation: past present and future, Carlos Coello, CIC, CINVESTAV, Mexico, (Shared with ENC 06)
13:30 – 14:00	Closing ceremony