



Conference Programme

Puebla, México
28 - 30 September, 2005

ReConFig'05	
Sept. 28, 2005	
8:00 - 9:00	Conference Registration
9:00 - 9:05	Opening Speech
9:05 - 10:45	Session 1 - Architectures 1. A Handel-C Implementation of the Back-Propagation Algorithm on Field Programmable Gate Arrays Vijay Pandya, Shawk Areebi and Medhat Moussa 2. Rapid Prototyping of a Self-Timed ALU with FPGAs Ortega-Cisneros S., Raygoza-Panduro J.J., Suardiaz Muro J., Boemo E. 3. An FPGA-based Parallel Sorting Architecture for the Burrows Wheeler Transform José Martínez, René Cumpido, Claudia Feregrino 4. Design and Implementation of an Embedded Microprocessor Compatible With IL Language in Accordance to the Norm IEC 61131-3 Snaider Camillo L., Agenor Polo Z., Mario Esmeral P.
10:45 - 11:00	Coffee Break
11:00 - 12:00	Talk 1 Vision Sensors using FPGAs Gerardo Sosa, National Institute for Astrophysics, Optics and Electronics
12:00 - 12:15	Coffee Break
12:15 - 14:00	Session 2 - Architectures and Image Processing 1. Real-Time FPGA-Based Architecture for Bicubic Interpolation: An Application for Digital Image Scaling Marco Aurelio Nuño-Maganda, Miguel-O Arias-Estrada 2. An Image Comparison Circuit Design Miguel Angel Sánchez Martínez and Adriano De Luca Pennacchia 3. FPGA-Based Customizable Systolic Architecture for Image Processing Applications Graciela Saldaña, Miguel Arias-Estrada 4. FPGA Implementation of a synchronous and self-timed neuroprocessor Raygoza-Panduro J.J., Ortega-Cisneros S., Boemo E.
14:00 - 16:00	Lunch break
16:00 - 17:40	Session 3 - Arithmetic 1. An FPGA Arithmetic Logic Unit for Computing Scalar Multiplication using the Half-Add Method Sabel Hernández-Rodríguez, Francisco Rodríguez-Henríquez 2. Hardware signal processing unit for one-dimensional variable-length discrete wavelet transform Ordaz-Moreno Alejandro, Romero-Troncoso Rene de Jesus, Vile-Frias Jose Alberto 3. VHDL Core for 1024-Point Radix-4 FFT Computation Vile-Frias Jose Alberto, Romero-Troncoso Rene de Jesus, Ordaz-Moreno Alejandro 4. FPGA Implementation of an efficient multiplier over finite fields GF(2 ^m) Mario Alberto García-Martínez, Rubén Posada-Gómez, Guillermo Morales-Luna, Francisco Rodríguez-Henríquez
17:40 - 18:00	Coffee Break
18:00 - 19:00	Keynote Speech 1 Reconciling Logic and Objects Robert Kowalski, Imperial College, UK
19:00 - 20:00	Official Opening
20:00 - 21:00	Toast and Cultural Event

ReConFig'05	
Sept. 29, 2005	
8:00 - 9:00	Conference Registration
9:00 - 9:05	Welcome Day 2
9:05 - 10:45	Session 4 - Reconfiguration 1. On the Design of Two-Level Reconfigurable Architectures Sebastian Lange, Martin Middendorf 2. A Secure Self-Reconfiguring Architecture based on Open Source Hardware Javier Castillo, Pablo Huerta, José Ignacio Martínez 3. Platform for Intrinsic Evolution of Analogue Neural Networks Patrick Rocke, John Maher, Fearghal Morgan 4. Dynamic Voting Schemes to Enhance Evolutionary Repair in Reconfigurable Logic Devices Corey J. Millard, C. A. Shama, R. F. DeMara
10:45 - 11:00	Coffee Break
11:00 - 12:00	Keynote Speech 2 High Performance Computing using Reconfigurable Hardware Viktor K. Prasanna, University of Southern California
12: - 12:15	Coffee Break
12:15 - 14:00	Session 5 - Physical Design 1. Design Space Exploration of Coarse-Grain Reconfigurable DSPs Martin Zabel, Steffen Köhler, Martin Zimmerling, Thomas B. Preußner, Rainer G. Spallek 2. Optimizing Register Binding in FPGAs Using Simulated Annealing Annie Avakian, Iyad Ouassif 3. Hierarchical FPGA clustering based on a multilevel partitioning approach to improve routability and reduce power dissipation Zed Marnakchi, Hayder Mraabet, Habib Mehrez 4. A novel FPGA Implementation of a Welding Control using a new Bus Architecture Rauma K., Luukko J., Häkkinen T., Pajari, I. and Pyhäönen O.
14:00 - 16:00	Lunch break
16:00 - 17:40	Session 6 - Tools 1. High quality uniform random number generation for massively parallel simulations in FPGAs David Thomas, Wayne Luk 2. VANNGen: a Flexible CAD Tool for Hardware Implementation of Artificial Neural Networks André Braga, Carlos Humberto Llanos, Mauricio Ayala-Rincón, Ricardo P. Jacobi 3. Quartz: A Framework for Correct and Efficient Reconfigurable Design Oliver Pail, Wayne Luk 4. Applied VHDL Training Methodology, EDA Framework and Hardware Implementation Platform Fearghal Morgan, Patrick Rocke, Martin O'Halloran
17:40 - 18:00	Coffee Break
18:00 - 19:00	Keynote Speech 3 Model Construction of Nonrigid Biological Objects from Images Dmitry Golod, University of South Florida
20:30	Dinner

ReConFig'05	
Sept. 30, 2005	
9:00 - 9:05	Welcome Day 3
9:05 - 10:45	Session 7 - Signal Processing 1. On the design of an FPGA-Based OFDM modulator for IEEE 802.16-2004 Joaquín García, René Cumpido 2. FPGA Implementation of DSV-PWM Modulator Ossi Laakkonen, Hannu Sarén, Kimmo Rauma, Olli Pyhäönen 3. An FPGA-based Coprocessor for the SPHINX Speech Recognition System: Early Experiences Guillermo Marcus, Juan A. Nolasco-Flores 4. Hardware/Software implementation of a Discrete Cosine Transform Algorithm Using SystemC A. Avila, R. Santoyo, S. O. Martinez, G. Dieck
10:45 - 11:00	Coffee Break
11:00 - 12:00	Keynote Speech 4 Topic TBA Alexander Gebuck, IPN Mexico
12: - 12:15	ReConFig Closing Toast and Awards

NOTE: Keynote Speeches are common to ReConFig and ENC. They will be open to attendees of both conferences.