Technical Program

2016 International Conference on ReConFigurable Computing and FPGAs

	Tuesday, November 29	
17:00 - 19:00	Registration	

	Wednesday, November 30	
08:30 - 17:00	Registration	
08:45 - 09:00	**Opening Session**	
09:00 - 10:00	**Keynote #1 - Growing the ReConFig Community through Python, Zynq and Hardware Overlays- Graham Schelle - Xilinx**	
10:00 - 10:15	Break	
10:15-11:45	**Session 1 - General 1**	
10:15-10:45	Lukas Johannes Jung and Christian Hochberger. Optimal Processor Interface for CGRA-based Accelerators Implemented on FPGAs	
10:45-11:15	Kledermon Garcia, Duarte Oliveira, Roberto d'Amore, Lester Faria and João Luis Oliveira. FPGA Implementation of Optimized XBM Specifications by Transformation for AFSMs	
11:15-11:45	Paolo Meloni, Deriu Gianfranco, Francesco Conti, Igor Loi, Luigi Raffo and Luca Benini. A high-efficiency runtime reconfigurable IP for CNN acceleration on a mid-range all-programmable SoC	
11:45-12:00	Break	
12:00-13:00	**Session 2 - General 2**	
12:00-12:30	Kentaro Orimo, Kota Ando, Kodai Ueyoshi, Masayuki Ikebe, Tetsuya Asai and Masato Motomura. FPGA Architecture for Feed-Forward Sequential Memory Network targeting Long-Term Time-Series Forecasting	
12:30-13:00	Natalia Nila-Olmedo, Fortino Mendoza-Mondragon and Alejandro Espinosa-Calderon. ARM+FPGA Platform to Manage Smart-Solid-State Transformer in Smart Grid Application	
13:00-14:30	Lunch	
14:30 - 16:00	**Session 3A - HPRC**	**Session 3B - DSP & Space**
14:30-15:00	Ali Asgar Sohanghpurwala and Peter Athanas. An Effective Probability Distribution SAT Solver on Reconfigurable Hardware	Hotaka Kusano, Masayuki Ikebe, Tetsuya Asai and Masato Motomura. An FPGA-Optimized Architecture of Anti-Aliasing based Super Resolution for Real-Time HDTV to 4K- and 8K-UHD Conversions
15:00-15:30	José Fonseca and João Canas Ferreira. An FPGA Implementation of a Long Short-Term Memory Neural Network	Tobias Lieske, Marc Reichenbach, Burkhard Ringlein and Dietmar Fey. Dataflow Optimization for Programmable Embedded Image Preprocessing Accelerators
15:30-16:00	Ernst Houtgast, Vlad-Mihai Sima, Giacomo Marchiori, Koen Bertels and Zaid Al-Ars. Power-Efficiency Analysis of Accelerated BWA-MEM Implementations on Heterogeneous Computing Platforms	Robért Glein, Florian Rittner and Albert Heuberger. Adaptive Single-Event Effect Mitigation for Dependable Processing Systems
16:00-16:30	Poster Introductions - Session A	Poster Introductions - Session B
16:30-17:15	**Poster Sessions A & B**	
19:00 - 21:00	**Welcome Cocktail & Demo Night**	

	Thursday, December 1
08:00 - 17:30	Registration
09:00 - 10:00	**Keynote #2 - FPGAs in the Datacenter – A Software View, Skip Booth - Cisco**
10:00 - 10:15	Break
	Session 4 - General 3
10:15-10:45	Thorbjörn Posewsky and Daniel Ziener. Efficient Deep Neural Network Acceleration through FPGA-based Batch Processing
10:45-11:15	Travis Haroldsen, Brent Nelson and Brad Hutchings. Packing a Modern Xilinx FPGA Using RapidSmith
11:15-11:45	Poster Introductions - Session C
11:45-12:30	**Poster Session C**
12:30-14:00	Lunch
14:00-13:30	**Session 5 - Networks and Communications**
14:00-14:30	Qianqiao Chen, Vaibhawa Mishra and Georgios Zervas. Reconfigurable Computing for Network Function Virtualization: A Protocol Independent Switch
14:30-15:00	Andreas Becher, Stefan Wildermann, Moritz Mühlenthaler and Jürgen Teich. ReOrder: Runtime Datapath Generation for High-Throughput Multi-Stream Processing
15:00-15:30	Jose Fernando Zazo, Sergio Lopez-Buedo, Gustavo Sutter and Javier Aracil. Automated synthesis of FPGA-based packet filters for 100 Gbps network monitoring applications
15:30-15:45	Break
15:45-17:45	**Session 6 - Security & Crypto**
15:45-16:15	Bernhard Jungk and Marc Stöttinger. Hobbit - Smaller But Faster Than A Dwarf: Revisiting Lightweight SHA-3 FPGA Implementations
16:15-16:45	Atil Utku Ay, Erdinc Ozturk, Erkay Savas and Francisco Rodríguez Henríquez. Design and Implementation of a Constant-time FPGA Accelerator for Fast Elliptic Curve Cryptography
16:45-17:15	Benjamin Buhrow, Barry Gilbert and William Goetzinger. 1 Tb/s Anti-Replay Protection with 20-port On-Chip RAM Memory in FPGAs
17:15-17:45	Wen Wang, Jakub Szefer and Ruben Niederhagen. Solving Large Systems of Linear Equations over GF(2) on FPGAs

19:45 - 23:00	**ReConFig Dinner**

	Friday, December 2	
09:30 - 11:00	Registration	
09:30-11:30	**Session 7A - NoC & RC Techniques**	**Session 7B - Productivity**
09:30-10:00	Sebastian Meisner and Marco Platzner. Thread Shadowing: On the Effectiveness of Error Detection at the Hardware Thread Level	Sam M.H. Ho, Maolin Wang, Ho-Cheung Ng and Hayden K.H. So. Towards FPGA-assisted Spark: An SVM Training Acceleration Case Study
10:00-10:30	Khaled Ahmed, Mohamed Rizk and Mohammed Farag. Overloaded CDMA Interconnect for Network-on-Chip (OCNoC)	Tobias Kalb and Diana Göhringer. Enabling Dynamic and Partial Reconfiguration in Xilinx SDSoC
10:30-11:00	Andreas Becher, Jutta Pirkl, Achim Herrmann, Jürgen Teich and Stefan Wildermann. Hybrid Energy-Aware Reconfiguration Management on Xilinx Zynq SoCs	Nam Khanh Pham, Akash Kumar and Khin Mi Mi Aung. Automatic Framework to Generate Reconfigurable Accelerators for Option Pricing Applications
11:00-11:30	Posters Introduction - Session D	Sen Ma and David Andrews. Breeze Computing: A Just In Time Approach for Virtualizing FPGAs in the Cloud
11:30:12:00		Posters Introduction - Session E
12:00 - 12:45	**Poster Sessions D & E**	
12:45 - 13:00	**Closing Remarks**	

Poster Session A

Paolo Di Febbo, Stefano Mattoccia and Carlo Dal Mutto. Real-Time Image Distortion Correction: Analysis and Evaluation of FPGA-Compatible Algorithms

Michail Vavouras and Christos Bouganis. Area-Driven Partial Reconfiguration for SEU Mitigation on SRAM-based FPGAs

Jan Moritz Joseph, Tobias Winker, Kristian Ehlers, Christopher Blochwitz and Thilo Pionteck. Hardware-Accelerated Pose Estimation for Embedded Systems using Vivado HLS

Steffen Vaas, Marc Reichenbach, Ulrich Margull and Dietmar Fey. The R2-D2 Toolchain - Automated Porting of Safety-Critical Applications to FPGAs

Thomas Preußer and Markus Krause. Survey on and Re-Evaluation of Wide Adder Architectures on FPGAs

Poster Session B

Nobuyuki Yahiro, Bo Liu, Atsushi Nanri, Yasuhiro Takashima, Shigetoshi Nakatake and Gong Chen. A Multi-functional Memory Unit with PLA-based Reconfigurable Decoder

Andres Jacoby and Daniel Llamocca. Dual Fixed-Point CORDIC Processor: Architecture and FPGA Implementation

Maolin Wang, Ho-Cheung Ng, Bob Man-Fung Chung, Sharat Chandra Varma Bogaraju, Manish Kumar Jaiswal, Sam M.H Ho, Kevin K. Tsia, Anderson Ho-Cheung Shum and Hayden Kwok-Hay So. High-throughput Cellular Imaging with High-Speed Asymmetric-Detection Time-Stretch Optical Microscopy under FPGA platform

Jaco Hofmann, Jens Korinth and Andreas Koch. A Scalable Latency-Insensitive Architecture for FPGA-Accelerated Semi-Global Matching in Stereo Vision Applications

Habib Ul Hasan Khan and Diana Goehringer. FPGA Debugging by a Device Start and Stop Approach

Poster Session C

Paul Rogers, Rajesh Kavasseri and Scott Smith. An FPGA-based design for joint control and monitoring of Permanent Magnet Synchronous Motors

Vaibhawa Mishra, Qianqiao Chen and Georgios Zervas. REoN: A Protocol for Reliable Software-Defined FPGA Partial Reconfiguration over Network

Mario Ruiz, Gustavo Sutter, Sergio Lopez-Buedo and Jorge E. Lopez de Vergara. FPGA-based encrypted network traffic discrimination at 100 Gb/s

Robert Karam, Tamzidul Hoque, Sandip Ray, Mark Tehranipoor and Swarup Bhunia. Robust Bitstream Protection in FPGA-based Systems through Low-Overhead Obfuscation

Farnoud Farahmand, Ekawat Homsirikamol and Kris Gaj. A Zynq-based testbed for the experimental benchmarking of algorithms competing in cryptographic contests

Florian Rittner, Robért Glein and Albert Heuberger. Detection and Isolation of Permanent Faults in FPGAs with Remote Access

Poster Session D

Gundolf Kiefer, Matthias Vahl, Julian Sarcher and Michael Schaeferling. A Configurable Architecture for the Generalized Hough Transform Applied to the Analysis of Huge Aerial Images

Matěj Bartík, Sven Ubik and Pavel Kubalík. A Novel and Efficient Method to Maintain FPGA Embedded Memory Content with an Asymptotically Constant Time (Re)Initialization Designed for an IP Packet Lossless Compression

Rasha Karakchi, Jordan Bradshaw and Jason Bakos. High-Level Synthesis of a Genomic Database Search Engine

Akihiko Hamada. Design and Implementation of Hardware Cache Mechanism and NIC for Column-Oriented Databases

Poster Session E

Thomas Preußer, Martin Zabel, Patrick Lehmann and Rainer G. Spallek. The Portable Open-Source IP Core and Utility Library PoC

Siavash Rezaei, Cesar-Alejandro Hernandez-Calderon, Saeed Mirzamohammadi, Eli Bozorgzadeh, Alexander Veidenbaum and Alex Nicolau. Data-rate-aware FPGA-based Acceleration of Streaming Applications

Jens Rettkowski, Konstantin Friesen and Diana Goehringer. RePaBit:Automated Generation of Relocatable Partial Bitstreams for Xilinx Zynq FPGAs

Thaddeus Koehn and Peter Athanas. Automating Structured Matrix-Matrix Multiplication for Stream Processing

Tiziana Fanni and Luigi Raffo. Coarse Grain Reconfiguration: Power Estimation and Management Flow for Hybrid Gated Systems