Technical Program

2015 International Conference on ReConFigurable Computing and FPGAs

	Sunday, Dec 6	
17:00 - 19:00	Registration	

	Monday, Dec 7	
08:00 - 17:30	Registration	
08:45 - 09:00	**Opening session**	
09:00 - 10:00	**Keynote #1 - Osker Mencer, CEO, CTO, Maxeler Technologies**	
10:00 - 10:15	Short Break	
10:15 - 11:30	**Session 1A - GS I**	**Session 1B - HPRC**
	Jens Rettkowski, Andrew Boutros and Diana Göhringer. Real-Time Pedestrian Detection on a Xilinx Zynq using the HOG Algorithm	Sven Hager, Daniel Bendyk and Björn Scheuermann. Partial Reconfiguration And Specialized Circuitry for Flexible FPGA-based Packet Processing
	Arif Irwansyah, Omar W. Ibraheem, Jens Hagemeyer, Mario Porrmann and Ulrich Rueckert. FPGA-based Circular Hough Transform with Graph Clustering for Vision-based Multi-Robot Tracking	Da Tong and Viktor Prasanna. High Throughput Sketch Based Online Heavy Change Detection on FPGA
	Sang-Woo Jun, Chanwoo Chung and Arvind. Large-scale high-dimensional nearest neighbor search using flash memory with in-store processing	Javier Alejandro Varela, Christian Brugger, Christian De Schryver, Norbert Wehn, Songyin Tang and Steffen Omland. Exploiting the Brownian Bridge Technique to improve Longstaff-Schwartz American Option Pricing on FPGA
11:30 - 12:00	Break	
12:00 - 13:40	**Session 2A - GS II**	**Session 2B - CGRAC**
	Ajitesh Srivastava, Ren Chen, Viktor K. Prasanna and Charalampos Chelmis. A Hybrid Design for High Performance Large-scale Sorting on FPGA	Anthony Brandon, Joost Hoozemans, Jeroen van Straten, Arthur Lorenzon, Anderson Sartor, Antonio Carlos Schneider Beck and Stephan Wong. A Sparse VLIW Instruction Encoding Scheme Compatible with Generic Binaries
	Ryan Pattison, Christian Fobel, Gary Gréwal and Shawki Areibi. Scalable Analytic Placement for FPGA on GPGPU	Carlo Sau, Luca Fanni, Paolo Meloni, Luigi Raffo and Francesca Palumbo. Reconfigurable Coprocessors Synthesis in the MPEG-RVC Domain
	Jose Fernando Zazo, Sergio Lopez-Buedo, Yury Audzevich and Andrew W. Moore. A PCIe DMA Engine to Support the Virtualization of 40 Gbps FPGA-Accelerated Network Appliances	Marc Reichenbach, Tobias Lieske, Steffen Vaas, Konrad Häublein and Dietmar Fey. FAUPU - A Design Framework for the Development of Programmable Image Processing Architectures
	Mohsen Ghasempour, Jonathan Heathcote, Javier Navaridas, Luis A. Plana, Jim Garside and Mikel Luján. Analysis of FPGA and Software Approaches to Simulate Unconventional Computer Architectures	
13:40 - 15:00	Lunch	
15:00 - 16:40	**Session 3A - GS III**	**Session 3B - PE & HLS**
	Lukas Johannes Jung and Christian Hochberger. Feasibility of High Level Compiler Optimizations in Online Synthesis	Joshua S. Monson and Brad Hutchings. Using Shadow Pointers to Trace C Pointer Values in FPGA Circuits

	Luis Contreras, Sérgio Cruz, J.M.S.T. Motta and Carlos H. Llanos. FPGA Implementation of the EKF Algorithm for Localization in Mobile Robotics using a Unified Hardware Module Approach	Sen Ma, Hongyuan Ding, Miaoqing Huang and David Andrews. Archborn: An Open Source Tool for Automated Generation of Chip Heterogeneous Multiprocessor Architectures
	Shijie Zhou, Charalampos Chelmis and Viktor K. Prasanna. Optimizing Memory Performance for FPGA Implementation of PageRank	Thaddeus Koehn and Peter Athanas. Buffering Strategies for Ultra High-Throughput Stream Processing
	Christopher Blochwitz, Jan Moritz Joseph, Rico Backasch, Stefan Werner, Dennis Heinrich, Sven Groppe and Thilo Pionteck. An Optimized Radix-Tree for Hardware-Accelerated Dictionary Generation for Semantic Web Databases	Sam Skalicky, Tejaswini Ananthanarayana, Sonia Lopez and Marcin Lukowiak. Designing Customized ISA Processors using High Level Synthesis
16:40 - 17:10	Posters introduction - Session A	Posters introduction - Session B
17:10 - 18:00	**Poster Sessions A & B**	
20:00 - 22:00	Welcome Cocktail & Demo night	

	Tuesday, Dec 8	
08:30 - 17:30	Registration	
09:00 - 10:00	**Keynote #2 - Gordon Chiu, Director, Software Engineering, Altera**	
10:00 - 10:15	Short Break	
10:15 - 11:30	**Session 4A - GS IV**	**Session 4B - DSP I**
	Giulia Gnemmi, Mattia Crippa, Gianluca Durelli, Riccardo Cattaneo, Gabriele Pallotta and Marco D. Santambrogio. On How to Efficiently Accelerate Brain Network Analysis on FPGA-Based Computing System	Jean Pierre David. Low Latency Solver for Linear Equation Systems in Floating Point Arithmetic
	Siddharth S. Bhargav, Rishvanth K. Prabakar and Young H. Cho. Accurate In-situ Runtime Measurement of Energy per Operation of System-on-Chip on FPGA	Omar W. Ibraheem, Arif Irwansyah, Jens Hagemeyer, Mario Porrmann and Ulrich Rueckert. A Resource-Efficient Multi-Camera GigE Vision IP Core for Embedded Vision Processing Platforms
11:05 - 11:30	Posters introduction - Session C	Posters introduction - Session D
11:30 - 12:00	**Poster sessions C & D**	
12:00 - 14:05	**Session 5A - MPSNoC**	**Session 5B - SC I**
	Bruno Silva, Alexandre Delbem, Vanderlei Bonato and Pedro Diniz. Runtime Mapping and Scheduling for Energy Efficiency in Heterogeneous Multi-Core Systems	Festus Hategekimana, Adil Tbatou, Christophe Bobda, Charles Kamhoua and Kevin Kwiat. Hardware Isolation Technique for IRC-based Botnets Detection
	Johanna Sepúlveda, Daniel Flórez and Guy Gogniat. Efficient and Flexible NoC-Based Group Communication for Secure MPSoCs	Henitsoa Rakotomalala, Xuan Thuy Ngo, Zakaria Najm, Jean-Luc Danger and Sylvain Guilley. Private Circuits II versus Fault Injection Attacks
	Pongstorn Maidee and Alireza Kaviani. Improving FPGA NoC Performance using Virtual Cut-Through Switching Technique	Stefan Gehrer, Sebastien Leger and Georg Sigl. Aging Effects on Ring-Oscillator-Based Physical Unclonable Functions on FPGAs

		Burak Erbagci, Mudit Bhargava, Rachel Dondero and Ken Mai. Deeply Hardware-Entangled Reconfigurable Logic and Interconnect
		Benjamin Buhrow, Karl Fritz, Barry Gilbert and Erik Daniel. A Highly Parallel AES-GCM Core for Authenticated Encryption of 400 Gb/s Network Protocols
14:05 - 16:30	Lunch & Break	
16:30 - 22:00	**Visit to Xcaret & Conference Dinner**	

	Wednesday, Dec 9	
09:00 - 11:30	Registration	
09:30 - 10:45	**Session 6A - DSP II**	**Session 6B - SC II**
	Hamza Bendaoudi, Qifeng Gan, Farida Cheriet, Houssem Ben Tahar and J. M. Pierre Langlois. A Run-Length Encoding Co-Processor for Retinal Image Texture Analysis	Maxime Lecomte, Jacques J.A. Fournier and Philippe Maurine. Thoroughly analyzing the use of Ring Oscillators for on-chip Hardware Trojan detection
	Thaddeus Koehn, Matthew Carrick and Peter Athanas. An Efficient Structure for Run-time Configuration of Synthesis and Channelizer Filter Banks	Ekawat Homsirikamol, William Diehl, Ahmed Ferozpuri, Farnoud Farahmand, Malik Umar Sharif and Kris Gaj. A Universal Hardware API for Authenticated Ciphers
10:20 - 10:45	Posters introduction - Session E	Posters introduction - Session F
10:45 - 11:15	**Poster sessions E & F**	
11:15 -12: 30	**Session 7A - RT**	**Session 7B - CPS**
	Hongyuan Ding and Miaoqing Huang. Achieving Energy-efficiency on MPSoCs: Performance and Power Optimizations	Alexander Boschmann, Andreas Agne, Linus Witschen, Georg Thombansen, Florian Kraus and Marco Platzner. FPGA-based Acceleration of High Density Myoelectric Signal Processing
	Enrico A. Deiana, Marco Rabozzi, Riccardo Cattaneo and Marco D. Santambrogio. A Multiobjective Reconfiguration-Aware Scheduler for FPGA-Based Heterogeneous Architectures	Pei Zhang, Aaron Mills, Joseph Zambreno and Phillip H. Jones. A Software Configurable and Parallelized Coprocessor Architecture for LQR Control
12:05 - 12:30	Amit Kulkarni, Robin Bonamy and Dirk Stroobandt. Power Measurements and Analysis for Dynamic Circuit Specialization	Timo Jaeschke, Patrick Imberg, Michael Zapke, Michael Huebner and Nils Pohl. Scalable Modular Hardware Platform for FPGA Based Industrial Radar Flowmeters
12:30 - 13:00	Posters introduction - Session G	Posters introduction - Session H
13:00 - 13:30	**Poster sessions G & H**	
13:30 - 13:45	**Closing remarks**	

Poster Session A
Joshua Mack, Sam Bellestri and Daniel Llamocca. Floating Point CORDIC-based Architecture for Powering Computation

Viorel Suse and Dan Ionescu. A Real-Time Reconfigurable Architecture for Face Detection
Andrew Bean, Nachiket Kapre and Peter Cheung. G-DMA: Improving Memory Access Performance for Hardware Accelerated Sparse Graph Computation
Vincent Mirian and Paul Chow. Evaluating Shared Virtual Memory in an OpenCL Framework for Embedded Systems on FPGAs

Poster Session B
Alfonso Rodriguez, Juan Valverde and Eduardo de la Torre. Design of OpenCL-Compatible Multithreaded Hardware Accelerators with Dynamic Support for Embedded FPGAs
Syed Waqar Nabi and Wim Vanderbauwhede. Using Type Transformations to Generate Program Variants for FPGA Design Space Exploration
Zhongyuan Zhao, Weiguang Sheng, NaiFeng Jing, Weifeng He and ZhiGang Mao. Resource-Saving Compile Flow for Coarse-Grained Reconfigurable Architectures
Javier Pérez, Aiman Alabdo, Gabriel J. Garcia, Jorge Pomares and Fernando Torres. FPGA-based visual control of robot manipulators using dynamic perceptibility

Poster Session C
M. Ruiz, G. Sutter, S. López-Buedo, J. Ramos, J. E. López de Vergara and J. Aracil. Leveraging Open Source Platforms and High-Level Synthesis for the Design of FPGA-Based 10 GbE Active Network Probes
Roberto de Lima, Jose Martinez-Carranza, Alicia Morales-Reyes and Rene Cumplido. Accelerating the Construction of BRIEF Descriptors Using an FPGA-based Architecture
Vincent Mirian and Paul Chow. UT-OCL: An OpenCL Framework for Embedded Systems Using Xilinx FPGAs
Andrew Powell and Dennis Silage. Statistical Performance of the ARM Cortex A9 Accelerator Coherency Port in the Xilinx Zynq SoC for Real-Time Applications

Poster Session D
L. Canché Santos, A. Castillo Atoche, J. Vázquez Castillo, O. Longoria Gándara, R. Carrasco Alvarez and J. Ortegón Aguilar. An Improved Hardware Design for Matrix Inverse based on Systolic Array QR Decomposition and Piecewise Polynomial Approximation
Carl Ahlberg, Fredrik Ekstrand, Mikael Ekström, Giacomo Spampinato and Lars Asplund. GIMME2 - an embedded system for stereo vision and processing of megapixel images with FPGA-acceleration
Poona Bahrebar and Dirk Stroobandt. Design and Exploration of Routing Methods for NoC-based Multicore Systems
Tiziana Fanni, Carlo Sau, Paolo Meloni, Luigi Raffo and Francesca Palumbo. Power Modelling for Saving Strategies in Coarse Grained Reconfigurable Systems

Poster Session E
Amit Kulkarni, Vipin Kizheppatt and Dirk Stroobandt. MiCAP: A custom Reconfiguration Controller for Dynamic Circuit Specialization
Juri Schmidt and Ulrich Brüning. openHMC - A Configurable Open-Source Hybrid Memory Cube Controller
Riccardo Cattaneo, Gabriele Pallotta, Donatella Sciuto and Marco D. Santambrogio. Explicitly Isolating Data and Computation in High Level Synthesis: the Role of Polyhedral Framework
Osama G. Attia, Alex Grieve, Kevin R. Townsend, Phillip Jones and Joseph Zambreno. Accelerating All-Pairs Shortest Path Using A Message-Passing Reconfigurable Architecture

Poster Session F
Vincent Migliore, Maria Méndez Real, Vianney Lapotre, Arnaud Tisserand, Caroline Fontaine and Guy Gogniat. Exploration of Polynomial Multiplication Algorithms for Homomorphic Encryption Schemes
Cedric Jayet-Griffon, M.-A. Cornelie, P. Maistri, Ph. Elbaz-Vincent and R. Leveugle. Polynomial Multipliers for Fully Homomorphic Encryption on FPGA
Subhadeep Banik, Andrey Bogdanov and Francesco Regazzoni. Exploring the Energy Consumption of Lightweight Blockciphers in FPGA
Michal Varchola, Milos Drutarovsky, Pavol Zajac and Marek Repka. Side Channel Attack on Multiprecision Multiplier Used in Protected ECDSA Implementation

Poster Session G
Zoltán Endre Rákossy, Axel Acosta-Aponte, Tobias G. Noll, Gerd Ascheid, Rainer Leupers and Anupam Chattopadhyay. Design and Synthesis of Reconfigurable Control-Flow Structures for CGRA
Rico Backasch, Gerald Hempel, Christopher Blochwitz, Stefan Werner, Sven Groppe and Thilo Pionteck. An Architectural Template for Composing Application Specific Datapaths at Runtime
Joost Hoozemans, Jens Johansen, Jeroen van Straten, Anthony Brandon and Stephan Wong. Multiple Contexts in a Multi-ported VLIW Register File Implementation
Koichiro Masuyama, Yu Fujita, Hayate Okuhara and Hideharu Amano. A 297MOPS/0.4mW Ultra Low Power Coarse-graind Reconfigurable Accelerator CMA-SOTB-2
Hongyuan Ding and Miaoqing Huang. Exploiting Hardware Abstraction for Hybrid Parallel Computing Framework

Poster Session H
Kevin Lee and Peter Athanas. Shape Exploration for Modules in Rapid Assembly Workflows
Nikhil Thomas, Andrew Felder and Christophe Bobda. Adaptive Controller Using Runtime Partial Hardware Reconfiguration for Unmanned Aerial Vehicles (UAVs)
Armando Astarloa, Marcelo Urbina, Naiara Moreira, Unai Bidarte and David Modrono. FPGA based nodes for Sub-microsecond Synchronization of Cyber-Physical Production Systems on High Availability Ring Networks
Hugo A. Andrade, Patricia Derler, John C. Eidson, Ya-Shian Li-Baboud, Aviral Shrivastava, Kevin Stanton and Marc Weiss. Towards a Reconfigurable Distributed Testbed to Enable Advanced Research and Development of Timing and Synchronization in Cyber-Physical Systems