2014 International Conference on ReConFigurable Computing and FPGAs

	Sunday, Dec 7	
17:00 - 19:00	Registration	
	Monday, Dec 8	
08:00 - 17:30	Registration	
08:45 - 09:00	**Opening session**	
09:00 - 10:00	**Keynote #1 - Edward A. Lee, U.C. Berkeley**	
10:00 - 10:15	Short Break	
10:15 - 11:30	**Session 1A - GS I**	**Session 1B - CPS**
	Deferring Accelerator Offloading Decisions to Application Runtime. Gavin Vaz, Heinrich Riebler, Tobias Kenter and Christian Plessl.	Design of an Attention Detection System on the Zynq-7000 SoC. Fynn Schwiegelshohn and Michael Hübner.
	An AWF Digital Spectrometer for a Radio Telescope. Hiroki Nakahara, Hiroyuki Nakanishi and Kazumasa Iwai.	An Architectural Approach for Reconfigurable Industrial I/O Devices. Daniel Kirschberger, Holger Flatt and Jürgen Jasperneite.
	Embedding FPGA Overlays into Configurable Systems-on-Chip: ReconOS meets ZUMA. Tobias Wiersema, Arne Bockhorn and Marco Platzner.	FPGA-based Design and Implementation of Direct Torque Control for Induction Machines. Mohammad A. Zare, Rajesh G. Kavasseri and Cristinel Ababei.
11:30 - 12:00	Break	
12:00 - 13:15	**Session 2A - GS II**	**Session 2B - MPSoC**
	Kernel-Centric Acceleration of High Accuracy Stereo-Matching. Tobias Kenter, Henning Schmitz and Christian Plessl.	Overloaded CDMA Bus Topology for MPSoC Interconnect. Khaled E. Ahmed and Mohammed M. Farag.
	A Power-Efficient Real-Time Architecture for SURF Feature Extraction. C. Wilson, P. Zicari, S. Craciun, P. Gauvin, E. Carlisle, A. George and H. Lam.	Adaptive and Reconfigurable Fault-tolerant Routing Method for 2D Networks-on-Chip. Poona Bahrebar and Dirk Stroobandt.
	FPGA design and implementation of a matrix multiplier based accelerator for 3D EKF SLAM. Daniel Törtei Tertei, Jonathan Piat and Michel Devy.	Automatic Cache Partitioning and Time-triggered Scheduling for Real-time MPSoCs. Gang Chen, Biao Hu, Kai Huang, Alois Knoll, Kai Huang, Di Liu and Todor Stefanov.
13:15 - 15:00	Lunch	
15:00 - 16:15	**Session 3A - CGRA**	**Session 3B - HPRC**
	Force-Directed Scheduling for Data Flow Graph Mapping on Coarse-Grained Reconfigurable Architectures. Alexander Fell, Zoltán Endre Rákossy and Anupam Chattopadhyay.	Enabling FPGA support in MATLAB based Heterogeneous Systems. Sam Skalicky, Tyler Kwolek, Sonia Lopez and Marcin Lukowiak.
	On the Performance and Energy Efficiency of FPGAs and GPUs for Polyphase Channelization. Vignesh Adhinarayanan, Thaddeus Koehn, Krzysztof Kepa, Wu-chun Feng and Peter Athanas.	Advanced Branch Predictors for Soft Processors. Di Wu and Andreas Moshovos.
	Area-Efficient Dynamically Reconfigurable Protocol-Processing Hardware for Access Network Communications SoC. Saki Hatta, Nobuyuki Tanaka and Satoshi Shigematsu.	Characterization of OpenCL on a Scalable FPGA Architecture. Shanyuan Gao and Jeremy Chritz.
16:15 - 16:50	Posters introduction - Session A	Posters introduction - Session B
16:50 - 17:30	**Poster Sessions A & B**	
20:00 - 22:00	Welcome Cocktail & Demo night	

	Tuesday, Dec 9	
08:30 - 17:30	Registration	
09:00 - 10:00	**Keynote #2 - Thomas Flatley, NASA Goddard Space Flight Center**	
10:00 - 10:15	Short Break	
10:15 - 11:30	**Session 4A - GS III**	**Session 4B - PE**
	PAMS: Pattern Aware Memory System for Embedded Systems. Tassadaq Hussain, Nehir Sonmez, Oscar Palomar, Osman Unsal, Adrian Cristal, Eduard Ayguadé, Mateo Valero and S. A. Gursal.	A Framework for Efficient Rapid Prototyping by Virtually Enlarging FPGA Resources. Shinya Takamaeda-Yamazaki and Kenji Kise.
	A Unified OpenCL-flavor Programming Model with Scalable Hybrid Hardware Platform on FPGAs. Hongyuan Ding and Miaoqing Huang.	TINCR - A CUSTOM CAD TOOL FRAMEWORK FOR VIVADO. Brad White and Brent Nelson.
11:05 - 11:30	Posters introduction - Session C	Posters introduction - Session D
11:30 - 12:00	**Poster sessions C & D**	
12:00 - 13:15	**Session 5A - GS IV**	**Session 5B - DSP I**
	Net Reordering and Multicommodity Flow Based Global Routing for FPGAs. Cristinel Ababei, Rajesh G. Kavasseri and Mohammad A. Zare.	High-Throughput Hash-based Online Traffic Classification Engines on FPGA. Vaibhav R. Gandhi, Yun R. Qu and Viktor K. Prasanna.
	Hardware/Software Infrastructure for ASIC Commissioning and Rapid System Prototyping. Peter Reichel and Jens Döge.	Hardware Task-Status Manager for an RTOS with FIFO Communication. Pavel G. Zaykov, Georgi Kuzmanov, Anca Molnos and Kees Goossens.
		Efficient FPGA-Based Implementation of a CAZAC Sequence Generator for 3GPP LTE. Felipe A. P de Figueiredo, Fabiano S. Mathilde, Fabbryccio A. C. M. Cardoso, Rafael M. Vilela and João Paulo Miranda.
13:15 - 15:00	Lunch	
15:00 - 16:00	**Keynote #3 - Jan Gray, Gray Research LLC**	
16:00 - 16:15	Short break	
16:15 - 17:05	**Session 6A - GS V**	**Session 6B - DSP II**
	Fast and Generic Hardware Architecture for Stereo Block Matching Applications on Embedded Systems. Konrad Häublein, Marc Reichenbach and Dietmar Fey.	Stochastically Computing Discrete Fourier Transform with Reconfigurable Digital Fabric. Yu Bai and Mingjie Lin.
	A Generic Pixel Distribution Architecture for Parallel Video Processing. Karim M. A. Ali, Rabie Ben Atitallah, Saïd Hanafi and Jean-Luc Dekeyser.	High-Performance FPGA Implementations of Volterra DFEs for Optical Fiber Systems. A. Emeretlis, G. Theodoridis and George - Othon Glentis.
17:45 - 23:30	**Conference Dinner**	

	Wednesday, Dec 10	
09:00 - 11:30	Registration	
09:30 - 10:45	**Session 7A - RT I**	**Session 7B - SC I**
	Improving Reconfiguration Speed for Dynamic Circuit Specialization using Placement Constraints. Amit Kulkarni, Tom Davidson, Karel Heyse and Dirk Stroobandt.	Can High-Level Synthesis Compete Against a Hand-Written Code in the Cryptographic Domain? A Case Study. Ekawat Homsirikamol and Kris Gaj.
	A Device-Agnostic Tool For Precomputing Legal Placements in Modular Design Flows. Ali Asgar Sohanghpurwala, Peter Athanas and Andrew Love.	High-Speed Implementation of bcrypt Password Search using Special-Purpose Hardware. Friedrich Wiemer and Ralf Zimmermann.
10:20 - 10:45	Posters introduction - Session E	Posters introduction - Session F
10:45 - 11:15	**Poster sessions E & F**	
11:15 -12: 30	**Session 8A - RT II**	**Session 8B - SC II**
	On Providing Scalable Self-healing Adaptive Fault-tolerance to RTR SoCs. Byron Navas, Johnny Öberg and Ingo Sander.	A Hardware-Assisted Proof-of-Concept for Secure VoIP Clients on Untrusted Operating Systems. Maik Ender, Gerd Düppmann, Alexander Wild, Thomas Pöppelmann and Tim Güneysu.
	Data path analysis for Dynamic Circuit Specialisation. Tom Davidson and Dirk Stroobandt.	A Systematic Study of Lightweight Hash Functions on FPGAs. Bernhard Jungk, Leandro Rodrigues Lima and Matthias Hiller.
12:05 - 12:30	Posters introduction - Session G	Posters introduction - Session H
12:30 - 13:10	**Poster sessions G & H**	
13:10 - 13:15	**Closing remarks**	

Poster Session A
Rotated Parallel Mapping: A Novel Approach for Mapping Data Parallel Applications on CGRAs. Simon Schulz, Oliver Bringmann, Thomas Schweizer and Wolfgang Rosenstiel.
Dynamic Protocol Stacks in Smart Camera Networks. Markus Happe, Yujiao Huang and Ariane Keller.
400 Gbps Energy-Efficient Multi-Field Packet Classification on FPGA. Shijie Zhou, Sihan Zhao and Viktor K. Prasanna.
Impact of defect tolerance techniques on the criticality of a SRAM-based Mesh of Cluster FPGA. Adrien Blanchardon, Roselyne Chotin-Avot, Habib Mehrez and Emna Amouri.
Memory Optimisation for Hardware Induction of Axis-parallel Decision Tree. Chuan Cheng and Christos-Savvas Bouganis.
An A-FPGA Architecture for Relative Timing Based Asynchronous Designs. Jotham Vaddaboina Manoranjan and Kenneth S. Stevens.

Poster Session B
Phenox: Zynq 7000 based quadcopter robot. Ryo Konomura and Koichi Hori.
Place Reservation Technique for Online Task Placement on a Multi-context Heterogeneous Reconfigurable Architecture. Quang Hoa LE , Emmanuel Casseau and Antoine Courtay.
3D-LeukoNoC: A Dynamic NoC Protection. Johanna Sepúlveda, Guy Gogniat, Daniel Flórez, Jean-Philippe Diguet, Cesar Pedraza and Marius Strum.
A high-level analysis of a multi-core vision processor using SystemC and TLM2.0. Jones Y. Mori and Michael Huebner.
RAR-NoC: A Reconfigurable and Adaptive Routable Network-on-Chip for FPGA-based Multiprocessor Systems. Jens Rettkowski and Diana Göhringer.
PoC-Align: An Open-Source Alignment Accelerator using FPGAs. Thomas B. Preußer, Oliver Knodel and Rainer G. Spallek.

Poster Session C
FSM Merging and Reduction for IP Cores Watermarking using Genetic Algorithms. Jorge Echavarria, Alicia Morales-Reyes, René Cumplido and Miguel A. Salido.
Energy-Efficient Histogram on FPGA. Andrea Sanny, Yi-Hua E. Yang and Viktor K. Prasanna.
What Limits the Operating Frequency of a Soft Processor Design. Kaveh Aasaraai and Andreas Moshovos.
Mission Control: A Performance Metric and Analysis of Control Logic for Pipelined Architectures on FPGAs. Sam Skalicky, Sonia Lopez, Marcin Lukowiak and Christopher Wood.
Context-Aware Resources Placement for SRAM-based FPGA to minimize Checkpoint/Recovery overhead. Sahraoui Fouad, Fakhreddine Ghaffari, Mohamed El Amine Benkhelifa and Bertrand Granado.

Poster Session D
Dynamic Run-time Hardware/Software Scheduling For 3D Reconfigurable SoC. Quang-Hai Khuat, Daniel Chillet and Michael Hübner.
Smart Employment of Circuit Redundancy to Effectively Counter Trojans (SECRET) in Third-Party IP Cores. Mohammed M. Farag and Mohammad A. Ewais.
Versatile Educational and Research Robotic Platform Based on Reconfigurable Hardware. Carlos Andres Lara-Niño, Cesar Torres-Huitzil and Jose Hugo Barron-Zambrano.
FPGA-Based Accelerator Development for Non-Engineers. David Uliana, Peter Athanas and Krzysztof Kepa.
Zero-Latency Datapath Error Correction Framework for Over-Clocking DSP Applications on FPGAs. Rui Policarpo Duarte and Christos-Savvas Bouganis.

Poster Session E
Identifying Homogenous Reconfigurable Regions in Heterogeneous FPGAs for Module Relocation. Rico Backasch, Gerald Hempel, Stefan Werner, Sven Groppe and Thilo Pionteck.
A Highly Flexible Reconfigurable System on a Xilinx FPGA. Tomáš Drahonovský, Martin Rozkovec and Ondrej Novák.
Parameterised FPGA Reconfigurations for Efficient Test Set Generation. Alexandra Kourfali, Elias Vansteenkiste and Dirk Stroobandt
A Hardware Generator for Factor Graph Applications. James Demma and Peter Athanas.
FPGA-Based Reconfigurable Unit for Real-Time Power Quality Index Estimation. Misael Lopez-Ramirez, Luis M. Ledesma-Carrillo, Ana L. Martínez-Herrera, Eduardo Cabal-Yepez and Homero Miranda-Vidales.

Poster Session F

TNT10G: A High-Accuracy 10 GbE Traffic Player and Recorder for Multi-Terabyte Traces. Jose Fernando Zazo, Marco Forconesi, Sergio Lopez-Buedo, Gustavo Sutter and Javier Aracil.

An FPGA-based all-digtal 802.11b & 802.15.4 receiver for the Software Defined Radio Paradigm. Alfredo Espinoza-Rhoton, Luis F. Gonzalez-Perez, J.L. Ponce, Hector Borrayo-S., Lennin C.-Yllescas, R. Parra-Michel and Hassan Aboushady.

A Practical Scheme for Implementing Dynamic Spectral Precoding in OFDM. Enrique Mariano Lizarraga and Graciela Corral-Briones.

Power Analysis Attack on Hardware Implementation of MAC-Keccak on FPGAs. Pei Luo, Yunsi Fei, Xin Fang, A. Adam Ding, Miriam Leeser and David R. Kaeli.

Side-channel Power Analysis of Different Protection Schemes Against Fault Attacks on AES. Pei Luo, Yunsi Fei, Liwei Zhang and A. Adam Ding.

Poster Session G - PhD Forum

A Conceptual Toolchain for an Application Domain Specific Reconfigurable Logic Architecture. Timm Bostelmann and Sergei Sawitzki.

An AXI Compatible Cypress EZ-USB FX3 Interface for USB-3.0 SuperSpeed. Benedikt Janßen, Michael Hübner and Timo Jaeschke.

Low Power RAM-Based Hierarchical CAM on FPGA. Zhuo Qian and Martin Margala.

FPGA implementation of a reconfigurable image encryption system. M.T. Ramírez-Torres, J. S. Murguía and M. Mejía-Carlos.

An Adaptive Victim Cache Scheme. Osvaldo Navarro and Michael Hübner.

A Hardware Architecture for Filtering Irreducible Testors. Vladímir Rodríguez, José F. Martínez, Jesús A. Carrasco, Manuel S. Lazo, René Cumplido and Claudia Feregrino Uribe.

The FPGA implementation of an image registration algorithm using binary images. An Hung Nguyen, Mark Pickering and Andrew Lambert.

Poster Session H

Spiking dynamic neural fields architectures on FPGA. Benoît Chappet de Vangel, Cesar Torres-Huitzil and Bernard Girau.

Enabling Partial Reconfiguration for Coprocessors in Mixed Criticality Multicore Systems Using PCI Express Single-Root I/O Virtualization. Duy Viet Vu, Oliver Sander, Timo Sandmann, Steffen Baehr, Jan Heidelberger and Juergen Becker.

LUT based Secure Cloud Computing - an Implementation using FPGAs. Lei Xu, Pham Dang Khoa, Seung Hun Kim, Won Woo Ro and Weidong Shi.

The speed-up of detection of space debris using “InterP” and “FLOPS2D”. Naoyuki Fujita, Toshifumi Yanagisawa, Hirohisa Kurosaki and Hiroshi Oda.