ReConFig 2012 Program

Tuesday, Dec. 4		
17:00 - 19:00	Registration	

Wednesday, Dec. 5		
08:00 - 17:30	Registration	
08:45 - 9:00	Opening	
9:00 - 10:00	Keynote #1: "The once and future FPGA: the confluence of configurable processing and reconfigurable technology", Grant Martin, Chief Scientist, Tensilica	
10:00 - 10:15	Short Break	
10:15 - 11:30	**Session 1A - GS I**	**Session 1B - HPRC I**
	"Eight Ways to put your FPGA on Fire – A Systematic Study of Heat Generators", Markus Happe, Hendrik Hangmann, Andreas Agne, Christian Plessl	"Evaluating Reconfigurable Dataflow Computing Using the Himeno Benchmark", Yukinori Sato, Yasushi Inoguchi, Wayne Luk, Tadao Nakamura
	"An Efficient and Scalable Architecture for Real-Time Distortion Removal and Rectification of Live Camera Images", Matthias Pohl, Michael Schaeferling, Gundolf Kiefer, Plamen Petrow, Egmont Woitzel, Frank Papenfuß	"Compact Trie Forest: Scalable architecture for IP Lookup on FPGAs", O˘uzhan Erdem, Aydin Carus, Hoang Le
	"Power-Efficient and Scalable Virtual Router Architecture on FPGA", Swapnil Haria, Thilan Ganegedara, Viktor Prasanna	"Efficient Reconfigurable Hardware Architecture for Accurately Computing Success Probability and Data Complexity of Linear Attacks", Andrey Bogdanov, Elif Bilge Kavun, Elmar Tischhauser, Tolga Yalçın
11:30 - 12:00	Break (Group photo)	
12:00 - 13:15	**Session 2A - RT I**	**Session 2B - DSP**
	"Heterogeneous Computer Architectures: An Image Processing Pipeline for Optical Metrology", Marc Reichenbach, Ralf Seidler, Dietmar Fey	"A Low Power Configurable SoC for Simulating Delay-based Audio Effects", Ling Liu, Jeremia Bär, Felix Friedrich, Jürg Gutknecht, Shiao-Li Tsao
	"Power Consumption Model for Partial and Dynamic Reconfiguration", Robin Bonamy, Daniel Chillet, Sébastien Bilavarn, Olivier Sentieys	"Hardware Design and Implementation of a Network-on-Chip Based Load Balancing Switch Fabric", Turhan Karadeniz, Lotfi Mhamdi, Kees Goossens, J.J. Garcia-Luna-Aceves
	"Dreams: A Tool for the design of Dynamically Reconfigurable Embedded and Modular Systems", Andrés Otero, Eduardo de la Torre, Teresa Riesgo	"FPGA-based Rapid Prototyping Platform for MIMO-BICM Design Space Exploration", Christina Gimmler-Dumont, Philipp Schläfer, Norbert Wehn
13:15 - 15:00	Lunch	
15:00 - 16:50	**Session 3A - SEC I**	**Session 3B - MPSoC I**
	"Automatic Generation of Identical Routing Pairs for FPGA Implemented DPL Logic", Wei He, Andrés Otero, Eduardo de la Torre, Teresa Riesgo	"A Multi-Core FPGA-Based SoC Architecture with Domain Segregation", Daniel Kliem, Sven-Ole Voigt
	"Efficient and Side-Channel Resistant Authenticated Encryption of FPGA Bitstreams", Andrey Bogdanov, Amir Moradi, Tolga Yalçın	"An Implementation of a Directory Protocol for a Cache Coherent System on FPGAs", Vincent Mirian, Paul Chow
	Poster Introduction - Session A	"Adapting Communication for Adaptable Processors: A Multi-Axis Reconfiguration Approach", Paulo C. Santos, Gabriel L. Nazar, Luigi Carro
		Poster Introduction - Session B
16:50 - 17:30	Poster Sessions A & B	
20:00 - 22:00	Welcome Cocktail & Demo night	

Thursday, Dec 6		
08:30 - 17:30	**Registration**	
09:00 - 10:00	Keynote #2: Jaime Cummins, CEO, Pico Computing	
10:00 - 10:15	**Short Break**	
10:15 - 11:30	**Session 4A - SEC II**	**Session 4B - MPSoC II**
	"Hardware Implementation of the GPS authentication", Mickaël Dardaillon, Cédric Lauradoux, Tanguy Risset	"Design of a Multi-Soft-Core based Laser Marking Controller", David Castells-Rufas, Oscar Vila-Closas, Jordi Carrabina
	"A FPGA-based scalable architecture for URL legal filtering in 100GbE networks", Jaime J. Garnica, Sergio Lopez-Buedo, Victor Lopez, Javier Aracil	"Reducing the Overall Cache Miss Rate Using Different Cache Sizes for Heterogeneous Multi-Core Processors", Bruno de Abreu Silva, Lucas Albers Cuminato and Vanderlei Bonato
	Poster Introduction - Session C	Poster Introduction - Session D
11:30 - 12:15	**Poster Sessions C & D**	
12:15 - 13:30	**Session 5A - GS II**	**Session 5B - RT II**
	"Static Voltage Over-scaling and Dynamic Voltage Variation Tolerance with Replica Circuits and Time Redundancy in Reconfigurable Devices", Dawood Alnajjar, Masanori Hashimoto, Takao Onoye, Yukio Mitsuyama	"A Novel Physical Defects Recovery Technique for FPGA-IP cores", Yuki Nishitani, Kazuki Inoue, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga, Toshinori Sueyoshi
	"Exploring Hardware Work Queue Support for Lightweight Threads in MPSoCs", Rahul R Sharma, Yamuna Rajasekhar, Ron Sass	"Resiliency-aware Scheduling for Reconfigurable VLIW Processors", Jeremy Abramson, Pedro C. Diniz
	"Determination of On-Chip Temperature Gradients on Reconfigurable Hardware", Carsten Tradowsky, Enrique Cordero, Thorsten Deuser, Michael Hübner, Jürgen Becker	"Module Relocation in Heterogeneous Reconfigurable Systems-on-Chip using the Xilinx Isolation Design Flow", L. Gantel, M.E.A Benkhelifa, F. Lemonnier, F. Verdier
13:30 - 15:00	**Lunch**	
15:00 - 16:00	Keynote #3: Eric Sivertson, President Quantum Trace	
16:00 - 16:15	**Short break**	
16:15 - 17:30	**Session 6A - GS III**	**Session 6B - HPRC II**
	"Robustness of Different TMR Granularities in Shared Wishbone Architectures on SRAM FPGA", U. Kretzschmar, A. Astarloa, J. Lázaro, M. Garay, J. Del Ser	"SPREX: A Soft Processor with Runahead Execution", Kaveh Aasaraai, Andreas Moshovos
	"A Lightweight Speculative and Predicative Scheme for Hardware Execution", Razvan Nane, Vlad-Mihai Sima, Koen Bertels	"Comparison of Processing Performance and Architectural Efficiency Metrics for FPGAs and GPUs in 3D Ultrasound Computer Tomography", Matthias Birk, Matthias Balzer, Nicole Ruiter, Juergen Becker
	"Optimizing Inter-FPGA Communication by Automatic Channel Adaptation", Johannes Romoth, Dirk Jungewelter, Mario Porrmann, Ulrich Rueckert, Jens Hagemeyer	"A Case Study of Streaming Storage Format for Sparse Matrices", Shweta Jain-Mendon, Ron Sass
19:45-22:30	**Conference Dinner**	

Friday, Dec 7	
09:30 - 10:50	**Session 7 - PE**
	"A Design Assembly Framework for FPGA Back-End Acceleration", Tannous Frangieh, Peter Athanas
	"Synchronized-Transfer-Level Design Methodology applied to Hardware Matrix Multiplication", Marc-Andre Daigneault, Jean Pierre David
	Poster Introduction - Session E
10:50 - 11:30	**Poster sessions E**
11:30 - 13:10	**Session 8 - GS IV**
	"An Automated Test Framework for Experimenting with Stochastic Behavior in Reconfigurable Logic", Alex Aa. Birklykke, Yannick Le Moullec, Lars K. Alminde, Ramjee Prasad
	"Multi-FPGA Prototyping Environment: Large Benchmark Generation and Signals Routing", Zied Marrakchi, Mariem Turki, Habib Mehrez
	"Fault mitigation by means of dynamic partial reconfiguration of Virtex-5 FPGAs", Andres Upegui, Julien Izui, Gilles Curchod
	"FPGA Embedded Single-cycle 16-bit Microprocessor and Tools", Luis Morales-Velazquez, Roque A. Osornio-Rios, Rene J. Romero-Troncoso
13:10 - 13:15	**Closing remarks**

Poster session A

"Efficient Parallel-Pipelined GHASH for Message Authentication", Karim M. Abdellatif, R. Chotin-Avot, H. Mehrez

"Two IP Protection Schemes for Multi-FPGA Systems", Lubos Gaspar, Viktor Fischer, Tim Güneysu, Zouha Cherif Jouini

"IPS ECCO: A Lightweight and Reconfigurable IPSec Core", Benedikt Driessen, Tim Güneysu, Elif Bilge Kavun, Oliver Mischke, Christof Paar, Thomas Pöppelmann

"Minimization of Average Execution Time Based on Speculative FPGA Configuration Prefetch", Adrian Lifa, Petru Eles and Zebo Peng

"A High-Performance Reconfigurable Computing Architecture using a Magnetic Configuration Memory", Victor Silva, Jorge R. Fernandes, Mário P. Véstias, Horácio C. Neto

Poster session B

"Developing Application-Specific Multiprocessor Platforms on FPGAs", Sen Ma, Miaoqing Huang, David Andrews

"A Heuristic-based Communication-aware Hardware Optimization Approach in Heterogeneous Multicore Systems", Cuong Pham-Quoc, Zaid Al-Ars, Koen Bertels

"A VLSI Architecture for the K-best Sphere-Decoder in MIMO Systems", Pedro Cervantes-Lozano, Luis F. González-Pérez, Andrés D. García-García

"An analytical approach for sizing of heterogeneous multiprocessor flexible platforms for iterative demapping and channel decoding", Vianney Lapôtre, Guy Gogniat, Jean-Philippe Diguet, Salim Haddad, Amer Baghdadi

"Dynamic Reconfiguration of Modular I/O IP cores for Avionic Applications", Venkatasubramanian Viswanathan, Rabie Ben Atitallah, Jean-Luc Dekeyser

Poster session C

"Design and Analysis of Layered Coarse-Grained Reconfigurable Architecture", Zoltán Endre Rákossy , Tejas Naphade, Anupam Chattopadhyay

"Optimizing the physical implementation of a reconfigurable cache", Santana Gil, A. D., Hernandez Calviño, M., Quiles Latorre, F. J., Herruzo Gómez, E., Benavides Benitez, J.I.

"A Memory Efficient IPv6 Lookup Engine on FPGA", Da Tong, Yi-Hua E. Yang, Viktor K. Prasanna

"A Methodology for the Design and Deployment of Reliable Systems on Heterogeneous Platforms", Hugo A. Andrade, Arkadeb Ghosal, Kaushik Ravindran, Brian L. Evans

"Versatile FPGA-based locomotion platform for legged robots", Jose Hugo Barron-Zambrano, Horacio Rostro-Gonzalez

Poster session D

"A Scalable Array for Cellular Genetic Algorithms: TSP as Case Study", Pedro Vieira dos Santos, José Carlos Alves, João Canas Ferreira

"Parallelization of the Estimation Algorithm of the 3D Structure Tensor", Ashraful Alam, Zain-ul-Abdin, Bertil Svensson

"A Novel Efficient FPGA Architecture for HMMER Acceleration", M.Nazrin M.Isa, Khaled Benkrid, Thomas Clayton

"An Implementation of 3D Electron Tomography on FPGAs", Frederik Grüll, Michael Kunz, Michael Hausmann, Udo Kebschull

"Akers's Wavefront Planner - One of the fastest Stencil-based Path Planners on FPGAs", Michael Schmidt, Dietmar Fey

Poster session E

"A Versatile UDP/IP based PC ↔ FPGA Communication Platform", Nikolaos Alachiotis, Simon A. Berger, Alexandros Stamatakis

"Facilitating IP Deployment in a Marte-Based MDE Methodology Using IP-XACT: A Xilinx EDK Case Study", G. Ochoa-Ruiz, O. Labbani-Narsis, E. Bourennane, S. Cherif, S. Meftali, J.-L. Dekeyser

"Isolation of Behavior Design from System Implementation", Andy Caley, Kent Gilson

"A Model Design of a 2560-Channel Neural Spike Detection Platform", Nashwa Elaraby, Iyad Obeid

"FPGA-based Testbed for Timing Behavior Evaluation of the Controller Area Network (CAN)", Tobias Ziermann, Alexander Butiu, Jürgen Teich, Daniel Ziener

"Pragma based parallelization - Trading hardware efficiency for ease of use?", Tobias Kenter, Henning Schmitz, Christian Plessl