2010 International Conference on Reconfigurable Computing and FPGAs, ReConFig10

Conference Program

December 13, Monday		
8:00 - 19:00	Registration	
8:45 - 9:00	Opening	
9:00 - 10:00	Keynote 1: "Enabling New Computational Frontiers using Reconfigurable Technology" by Tony Brewer, Chief Technology Officer and Co-Founder of Convey Computer Corporation	
10:00 - 10:15	Short Break	
10:15 - 11:30	Parallel Session GS1: General Session 1 GS1_1: "A Minimalistic Architecture for Reconfigurable WFS-Based Immersive-Audio", Dimitris Theodoropoulos, Georgi Kuzmanov and Georgi Gaydadjiev GS1_2: "MARC: A Many-Core Approach to Reconfigurable Computing", Ilia Lebedev, Shaoyi Cheng, Austin Doupnik, James Martin, Christopher Fletcher, Daniel Burke, Mingjie Lin and John Wawrzynek GS1_3: "Intrinsic identification of Xilinx Virtex-5 FPGA devices using uninitialized parts of configuration memory space", Oliver Sander, Benjamin Glas, Lars Braun, Juergen Becker and Klaus Mueller-Glaser	Parallel Session GS2: General Session 2 GS2_1: "An Efficient Non-Blocking Data Cache for Soft Processors", Kaveh Aasaraai and Andreas Moshovos GS2_2: "Runtime Task Mapping Based on Hardware Configuration Reuse", Kamana Sigdel, Mark Thompson, Carlo Galuzzi, Andy D. Pimentel, Koen Bertels GS2_3: "Modeling and formal control of partial dynamic reconfiguration", Sébastien Guillet, Florent Frizon de Lamotte, Eric Rutten, Guy Gogniat and Jean-Philippe Diguet
11:30 - 12:00	Coffee Break	
12:00 - 13:15	Parallel Session RT: Reconfiguration Techniques RT_1: "Using Partial Reconfiguration in an Embedded Message-Passing System", Manuel Saldana, Arun Patel, Hao Jun Liu and Paul Chow RT_2: "Run-time reconfiguration for automatic hardware/software partitioning", Tom Davidson, Karel Bruneel and Dirk Stroobandt RT_3: "Synthesis and Implementation of Hierarchical Finite State Machines with Implicit Modules", Valery Sklyarov, Iouliia Skliarova, Dmitri Mihhailov and Alexander Sudnitson	Parallel Session CPS: Cyber Physical Systems and Image Processing CPS_1: "An optimized FPGA Implementation for a Parallel Path Planning Algorithm based on Marching Pixels", Michael Schmidt and Dietmar Fey CPS_2: "Open Source Precision Timed Soft Processor for Cyber Physical System Applications", Stephen Craven, Jason Smith and Daniel Long CPS_3: "Mapping of a Real-Time Object Detection Application onto a Configurable RISC/Coprocessor Architecture at Full HD Resolution", Holger Flatt, Holger Blume and Peter Pirsch
13:15 - 15:00	Lunch	
15:00 - 16:15	Session GS3: General Session 3 GS3_1: "Fault Injection Results of Linux Operating on an FPGA Embedded Platform", Joshua Monson, Brad Hutchings and Mike Wirthlin GS3_2: "gNOSIS: A Board-level Debugging and Verification Tool", Md Khan, Richard Pittman and Alessandro Forin GS3_3: "Communication Architectures for Run-Time Reconfigurable Modules in a 2-D Mesh on FPGAs", Jochen Strunk, Johannes Hiltscher, Wolfgang Rehm and Heiko Schick	

16:15 - 16:50	Introduction to Poster Session 1	
16:50 - 17:20	Coffee Break & Poster Session 1	
17:20 - 19:00	Parallel Session GS4: General Session 4 GS4_1: "Hardware Particle Swarm Optimization based on the Attractive-Repulsive Scheme for Embedded Applications", Daniel Mauricio Muñoz, Carlos Humberto Llanos, Leandro Coelho and Mauricio Ayala-Rincón GS4_2: "Pl+A2acing Streaming Applications with Similarities on Dynamically Partially Reconfigurable Architectures", Stefan Wildermann, J. Angermeier, Eugen Sibirko and Jürgen Teich GS4_3: "Pruning the Design Space for Just-In-Time Processor Customization", Mariusz Grad and Christian Plessl GS4_4: "Cascading Deep Pipelines to Achieve High Throughput in Numerical Reduction Operations", Mingjie Lin and John Wawrzynek	Parallel Session MPSOC1: Multiprocessor Systems and Networks on Chip 1 MPSOC1_1: "Efficient Congestion-oriented Custom Network-on-Chip Topology Synthesis", Cristinel Ababei MPSOC1_2: "Merging Programming Models and On-Chip Networks to Meet the Programmable and Performance Needs of Multi-Core Systems on a Programmable Chip", Andrew Schmidt, William Kritikos, Erik Anderson, Ron Sass and Matt French MPSOC1_3: "A Hybrid Router Combining SDM-Based Circuit Switcing With Packet Switching for On-Chip Networks", Angelo Kuti Lusala MPSOC1_4: "Network processing in Multi-core FPGAs with Integrated Cache-Network Interface", Christoforos Kachris

December 14, Tuesday	
8:30 - 19:00	Registration
9:00 - 10:00	Keynote 2: "Advances and Challenges in Reconfigurable Computing" by John Wawrzynek, University of California Berkeley
10:00 - 10:15	Short Break
10:15 - 11:05	Session SC1: Reconfigurable Computing for Security and Cryptography 1 SC1_1: "Analysis and Enhancement of Ring Oscillators Based Physical Unclonable Functions in FPGAs", Crina Costea, Florent Bernard, Viktor Fischer and Robert Fouquet SC1_2: "Cross-correlation Cartography", Laurent Sauvage, Sylvain Guilley, Florent Flament, Jean-Luc Danger and Yves Mathieu
11:05 - 11:30	Introduction to Poster Session 2
11:30 - 12:00	Coffee Break & Poster Session 2
12:00 - 13:15	Session SC2: Reconfigurable Computing for Security and Cryptography 2 SC2_1: "Investigation of DPA Resistance of Block RAMs in FPGAs", Shaunak Shah, Rajesh Velegalati, Jens-Peter Kaps and David Hwang SC2_2: "HCrypt: A Novel Reconfigurable Crypto-processor with Secured Key Management", Lubos Gaspar, Viktor Fischer, Florent Bernard and Pascal Cotret SC2_3: "Quantitative and Statistical Performance Evaluation of Arbiter Physical Unclonable Functions on FPGAs", Yohei Hori, Takahiro Yoshida, Toshihiro Katashita and Akashi Satoh

13:15 - 15:00	Lunch
15:00 - 16:15	Session HPRC: High Performance Reconfigurable Computing HPRC_1: "A New Hardware Efficient Inversion Based Random Number Generator for Non-Uniform Distributions", Christian de Schryver, Daniel Schmidt, Norbert Wehn, Elke Korn, Ralf Korn and Henning Marxen HPRC_2: "Performance analysis of Hardware/Software Middleware in Network of Smart Camera Systems", Ali Akbar Zarezadeh and Christophe Bobda HPRC_3: "Fixed-Point Arithmetic Error Estimation in Monte-Carlo Simulations", Xiang Tian and Khaled Benkrid
16:15 - 16:50	Introduction to Poster Session 3
16:50 - 17:20	Coffee Break & Poster Session 3
17:20 - 19:00	Session DSP: Reconfigurable Computing for DSP and Communications DSP_1: "Implementing The Blue Midnight Wish Hash Function on Xilinx Virtex-5 FPGA Platform", Mohamed Aly, Martin Margala, Mohamed El-Hadedy and Svein J. Knapskog DSP_2: "Singular Value Decomposition Hardware for MIMO: State of the Art and Custom Design", Kevin Cunningham, Yue Wang, Prawat Nagvajara and Jeremy Johnson DSP_3: "FPGA Implementation of Adjustable Wideband Fractional Delay FIR Filters", Guillermo Ramirez-Conejo, Javier Diaz-carmona, Jose Delgado-Frias and Alfredo Padilla-Medina
20:00 - 22:30	Conference Dinner

December 15, Wednesday	
8:30 - 11:00	Registration
9:00 - 10:40	Session GS5: General Session 5 GS5_1: "Applying Model-Checking to Post-Silicon-Verification: Bridging the Specification-Realisation Gap", Ouiza Dahmoune and Robert de B. Johnston GS5_2: "A Dynamically Reconfigured Network Platform for High-Speed Malware Collection", Sascha Muehlbach and Andreas Koch GS5_3: "Design and Implementation of a Visual Fuzzy Control in FPGA for the Ball and Plate System", Marco Antonio Moreno Armendáriz, Elsa Rubio and Cesar Aaron Perez Olvera GS5_4: "FPGA-based Platform Development for Change Detection in GTAW Welding Process", Ronald H. Hurtado, Sadek C. A. Alfaro and Carlos H. Llanos
10:40 - 11:15	Introduction to Poster Session 4
11:15 - 12:00	Coffee Break & Poster Session 4
12:00 - 13:40	Session MPSOC2: Multiprocessor Systems and Networks on Chip 2 MPSOC2_1: "A cost-effective solution to increase system reliability and maintain global performance under unreliable silicon in MPSoC", Nicolas Hebert, Gabriel Marchesan Almeida, Pascal Benoit, Gilles Sassatelli and Lionel Torres

	MPSOC2_2: "Low Power Dual Core Microcontroller", Rajesh Kannan Megalingam, Ashwin Mohan, Shekhil Hassan Thavalengal, Tanmay Muralidhar Rao and Vivek Periye MPSOC2_3: "A Process-Oriented Streaming System Design Paradigm for FPGAs", Ling Liu and Oleksii Morozov MPSOC2_4: "Providing Better Multi-Processor Systems-on-Chip Resources Utilization by Means of Using a Control-Loop Feedback Mechanism", Gabriel Marchesan Almeida, Rémi Busseuil, Sameer Varyani, Nicolas Hébert, Gilles Sassatelli, Pascal Benoit, Lionel Torres and Michel Robert.
13:40 - 14:00	Closing

Poster Session 1

P1_1: "An Application Example of a Run-time Reconfigurable Embedded System", Daniel Kriesten, Volker Pankalla and Ulrich Heinkel

P1_2: "UCORE: Reconfigurable Platform for Educational Purposes", Francisco Javier Quiles, Manuel Ortiz, Maria Brox Jimenez, Carlos Diego Moreno, Javier Hormigo and Julio Villalba

P1_3: "A Two Level Architecture for high throughput DCT-Processor and Implementing on FPGA", Azad Fakhari and Mahmood Fathy

P1_4: "Parallel FPGA-based Implementation of Recursive Sorting Algorithms", Dmitri Mihhailov, Valery Sklyarov, Iouliia Skliarova and Alexander Sudnitson

P1_5: "Analysis and Preliminary Measurements of Radiated Emissions in an Asynchronous System versus its Synchronous Counterpart", Rui de Cristo, Ricardo Jasinski and Volnei Pedroni

P1_6: "Reconfigurable Digital Audio Mixer for Electroacoustic Music", David Branco, Iouliia Skliarova and José Vieira

P1_7: "A Hardware Architecture of an XML/XPath Broker for Content-Based Publish/Subscribe Systems", Fadi El-Hassan and Dan Ionescu

P1_8: "A Runtime Profiler: Toward Virtualization of Polymorphic Computing Platforms", Hamid Mushtaq, Mojtaba Sabeghi and Koen Bertels

P1_9: "Improving the Reliability of a FPGA using Fault-Tolerance Mechanism Based on Magnetic Memory (MRAM)", Luís Vitório Cargnini, Yoann Guillemenet, Lionel Torres and Gilles Sassatelli

Poster Session 2

P2_1: "High-Speed FPGA-Based Pseudorandom Generators with Extremely Long Periods", Mieczyslaw Jessa and Michal Jaworski

P2_2: "Skein Tree Hashing on FPGA", Marcin Lukowiak and Aric Schorr

P2_3: "Unfolding Method for Shabal on Virtex-5 FPGAs: Concrete Results", Julien Francq and Céline Thuillet

P2_4: "Evaluation of white-box and grey-box Noekeon implementations in FPGA", Zouha Cherif, Florent Flament, Shivam Bhasin, Jean-Luc Danger, Sylvain Guilley and Hervé Chabanne

P2_5: "On FPGA-based implementations of the SHA-3 candidate Grøstl", Bernhard Jungk and Steffen Reith

P2_6: "An Improved GF(2) Matrix Inverter with Linear Time Complexity", Ricardo Jasinski, Volnei Pedroni, Antonio Gortan and Walter Godoy Jr.

P2_7: "Accelerating 2D FFT with non-power-of-two problem size on FPGA", wendi wang, bo duan, chunming zhang, peiheng zhang and ninghui sun

P2_8: "Parallel data sort using networked FPGAs", Janardhan Singaraju and John Chandy

P2_9: "Issues on Building an MPI cluster on MicroBlaze", Juan-Carlos Díaz-Martín, Rico-Gallego Juan-Antonio, Carolina Gómez-Tostón Gutiérrez and Álvaro Cortés-Fácila

Poster Session 3

P3_1: "Modeling and Simulation of Reconfigurable Processors in Grid Networks", Muhammad Faisal Nadeem, Mahmood Ahmadi, Muhammad Nadeem and Stephan Wong

P3_2: "Accelerating Texture Features Extraction Algorithm using FPGA Architecture", Asadollah Shahbahrami and Alireza Akoshide

P3_3: "Huffman Coding-Based Compression Unit for Embedded Systems", Marco Antonio Soto Hernández, Oscar Alvarado-Nava and Francisco Javier Zaragoza Martínez

P3_4: "FPGA-Based Online Detection of Multiple-Combined Faults through Information Entropy and Neural Networks", Eduardo Cabal-Yepez, Ricardo Saucedo-Gallaga, Armando Garcia-Ramirez, Arturo Fernandez-Jaramillo, Marcos Pena-Anaya and Martin Valtierra-Rodriguez

P3_5: "Reconfigurable Cache implemented on an FPGA", David Ariel Santana Gil, José Ignacio Benavides Benítez, Manuel Hernández Calviño and Ezequiel Herruzo Gómez

P3_6: "Hardware Computation of the PageRank Eigenvector", Seamas McGettrick and Dermot Geraghty

P3_7: "A Hardware-Efficient Frequency Domain Correlator Architecture For Acquisition Stage in GPS", Eduardo Romero, Ramon Parra, Omar Longoria and Mariano Aguirre

P3_8: "Flex-SURF: A Flexible Architecture for FPGA-based Robust Feature Extraction for Optical Tracking Systems", Michael Schäferling and Gundolf Kiefer

P3_9: "Configuration Sharing Optimized Placement and Routing", Piotr Stepien and Jon Cobb

Poster Session 4

P4_1: "A Novel Hardware Implementation of the Compact Genetic Algorithm", Marco Antonio Moreno Armendáriz, Nareli Cruz Cortés and Alejandro León

P4_2: "Hardware Pessimistic Run-Time Profiling for A Self-Reconfigurable Embedded Processor Architecture", Shady O. Agwa, Hany H. Ahmad and Awad I. Saleh

P4_3: "Multi-channel driving systems for therapeutic applications based-on focused ultrasound", Javier Pindter-Medina, Andres David Garcia-Garcia, Samuel Pichardo, Laura Curiel and Jesus Enrique Chong-Quero

P4_4: "Reconfigurable node processing unit for a low-power wireless sensor network", Luis A Vera-Salas, Sandra V Moreno-Tapia, Roque A Osornio-Rios and Rene de J Romero-Troncoso

P4_5: "Genetic Algorithms and Artificial Neural Networks to Combinational Circuit Generation on Reconfigurable Hardware", Bruno Silva, Maurício Dias, Jorge Silva and Fernando Osório

P4_6: "FPGA Implementation of OFDM Transceiver for a 60GHz Wireless Mobile Radio System", Khaled Sobaihi, Akram Hammoudeh and David Scammell

P4_7: "Operating System Structures for Multiprocessor Systems on Programmable Chip", Miaoqing Huang, David Andrews and Jason Agron

P4_8: "R2NoC : dynamically Reconfigurable Routers for flexible Networks on Chip", Ludovic Devaux, Sébastien Pillement, Daniel Chillet and Didier Demigny

P4_9: "Power Consumption Calculation of AP-DCD Algorithm Using FPGA Platform", Sasmita Deo